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SUBJECT CODE : 3110016

DECODE

GTU - 2018 Syllabus
Semester-II
[CE/EE/EC/IT/CSE/Elex.]

BASIC ELECTRONICS

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FEATURES

- ☑ Covers Entire Syllabus
- ☑ Question Answer Format
- ☑ Exact Answers and Solutions
- ☑ Important Points to Remember
- ☑ Memory Map
- ☑ Solved Model Question Paper [As Per R-18 Pattern]
- ☑ Short Questions and Answers

SYLLABUS
BASIC ELECTRONICS (3110016)

1. **Diode theory and applications** : Basic idea about forward bias, reverse bias and VI characteristics, ideal diode, second and third approximation, surface mount diodes, Zener diode, Testing of diode with multi-meter, half wave rectifier, full wave rectifier, bridge rectifier, RC and LC filters, Design of un-regulated DC power supply, Clipping circuit, Clamping circuit, voltage multiplier circuit, Reading datasheet of semiconductor diode.**(Chapter - 1)**

2. **Bipolar junction transistors and its biasing** : BJT operation, BJT voltages and currents, CE, CB and CC characteristics, DC load line and bias point, base bias, emitter feedback bias, collector feedback bias, voltage divider bias, Thermal stability, biasing BJT switching circuits, transistor power dissipation and switching time, Testing of bipolar junction transistor with multi-meter, Reading datasheet of BJT. **(Chapter - 2)**

3. **Special purpose diodes and transistors** : Light emitting diode (LED), Zener diode, Zener diode circuit for voltage regulation, Photo diode, Solar cell, PIN diode, Varactor, Schottky diode, Varistors, Tunnel diode, Seven Segment display, Sixteen segment display, Identify segments on pin using multi-meter, Dot-matrix LED display, Photo transistor, Opto-coupler, Reading datasheet of opto-electronics devices **(Chapter - 3)**

4. **AC Analysis of BJT circuits and small signal amplifier** : Coupling and bypass capacitors, AC load lines, Transistor models and parameters, Common emitter circuit analysis, common base circuit analysis, common collector circuit analysis, Comparison of CE, CB and CC circuits, Transistor as a switch. **(Chapter - 4)**

5. **Field effect transistors (FET) and its biasing** : Junction field effect transistors(JFET), Comparison of BJT and FET, JFET characteristics, FET, Biasing in ohmic region and active region, Trans-conductance, amplification and switching, MOSFETs (D-type and E-type MOSFET), CMOS introduction, E-MOSFET amplifier, MOSFET testing, Reading datasheet for FET and MOSFET. **(Chapter - 5)**

6. **Digital Circuits** : Basic gates AND, OR,NOT, NAND, NOR, EX-OR, EX-NOR, Building AND, OR Gate with diodes, Digital logic families RTL, DTL, TTL, CMOS, Comparison of logic families **(Chapter - 6)**

TABLE OF CONTENTS

1 Diode

1.1 : P-N Junction

Q.1 What is p-n junction ?

Ans. : The two types of extrinsic materials are p type and n type.

- The p type and n type materials are chemically combined with a special fabrication technique to form p-n junction.
- On p-side there are large number of holes while on n-side there are large number of free electrons.

1.2 : Theory of P-N Junction

Q.2 Discuss the behaviour of p-n junction under no bias.

Ans. : • In a unbiased p-n junction diode, on p-side there are large number of holes while on n-side there are large number of electrons. Hence the overall there is nonuniform distribution of charge carriers.

- When such nonuniform distribution exists then the charge carriers start moving from high concentration area towards the low concentration area. This is called **diffusion.**
- In unbiased diode, the majority holes on p side start diffusing into n side while the majority free electrons on n side start diffusing into p side.
- In n region, the holes diffusing from p-side, recombine with free electrons. Thus due to additional positively charged holes, these atoms on n-side become **positive immobile ions**, just near the junction in n region.

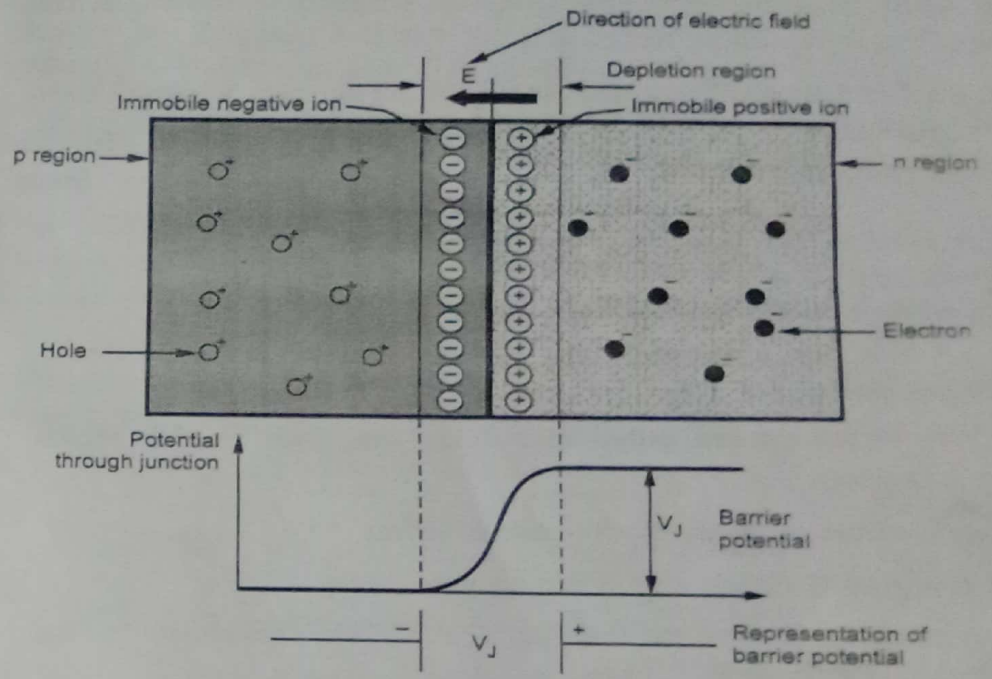


Fig. Q.2.1 The unbiased diode

- In p region, the free electrons diffusing from n-side, recombine with the holes of the atoms. Thus due to gain of additional negatively charged free electrons, these atoms become **negative immobile ions**, just near the junction in p-region.
- As more holes diffuse on p side, large immobile positive charge accumulates near the junction on n side. This positive charge repels the positively charged holes and the diffusion of holes stops.
- Similarly large negative charge accumulates near the junction on p side. This negative charge repels the negatively charged electrons and the diffusion of electrons stops.
- Thus there exists a wall near the junction with negative immobile charge on p side and positive immobile charge on n side. There are no charge carriers in this region. The region is depleted off

or **space charge region**. The depletion region is shown in the Fig. Q.2.1.

- In equilibrium condition, the depletion region gets widened upto a point where no further electrons or holes can cross the junction. Thus it acts as a **barrier**.

1.3 : P-N Junction Diode

Q.3 Explain p-n junction diode.

Ans. : • The p-n junction forms a popular semiconductor device called **p-n junction diode**.

- Its two terminals are called electrodes, one each from p region and n region.
- It can conduct current only in one direction.
- The p region is anode and n region is cathode.
- Its symbol is shown in the Fig. Q.3.1. The arrowhead in the symbol indicates the direction of the conventional current which can flow when an external voltage is applied in a specific manner across the diode.

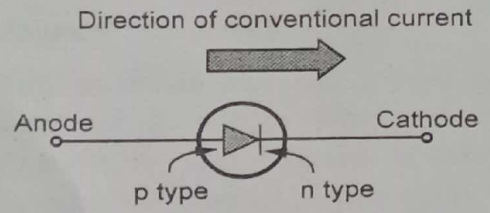


Fig. Q.3.1 Symbol of a diode

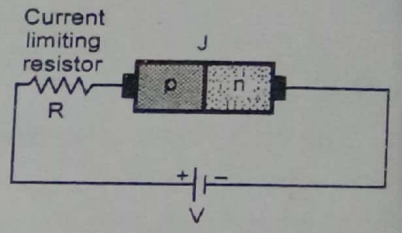
- Applying external voltage to p-n junction diode is called biasing.
- Depending upon the polarity of external d.c. voltage applied to diode, the biasing is classified as,

1. Forward biasing 2. Reverse biasing.

1.4 : Forward Biasing of Diode

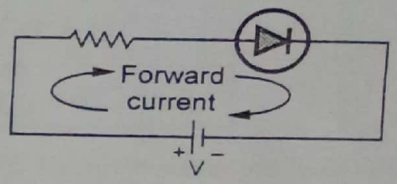
Q.4 Explain the forward biasing of p-n junction diode.

Ans. : • When an external d.c. voltage is connected in such a w that p region is connected to positive and n region to negative the d.c. voltage then the biasing is called **forward biasing**. It is shown in the Fig. Q.4.1.



(a) Forward biasing

- As long as applied voltage V is less than barrier potential there is no conduction.
- When applied voltage V is more than barrier potential, it overcomes the barrier potential and reduces the width of depletion region. This is because the negative of battery pushes the free electrons against the barrier from n to p region while positive of battery pushes holes against barrier from p to region.



(b) Symbolic representation

Fig. Q.4.1

- As applied voltage is increased, at a particular value, th depletion region becomes very narrow and majority charg carriers can easily cross the junction.
- This large number of majority charge carriers constitute a curren called **forward current**.
- The current in the p region is due to movement of holes so it i **hole current**. The current in the n region is due to movement o electrons so it is **electron current**. The holes in p region and electrons in n region are majority charge carriers. Hence the forward current is due to **majority charge carriers**.
- The forward current in a diode is shown in the Fig. Q.4.2.

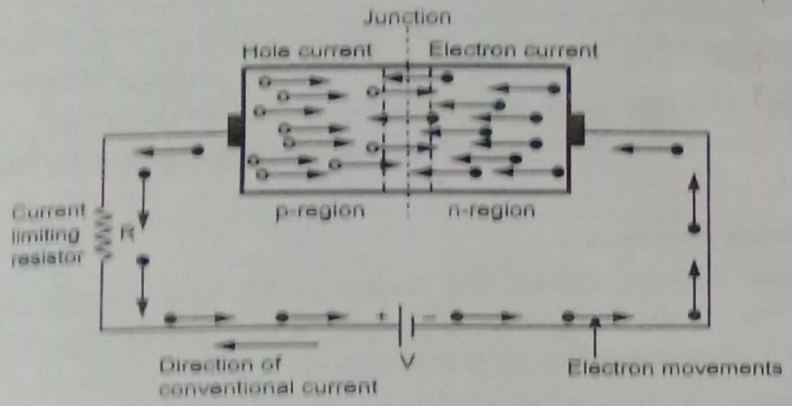
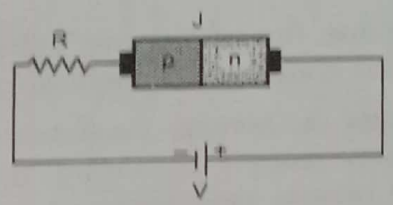


Fig. Q.4.2 Forward current in a diode

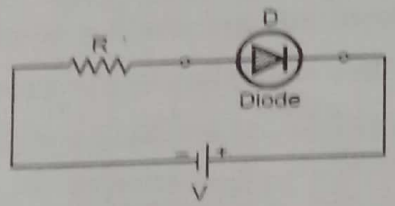
1.5 : Reverse Biasing of Diode

Q.5 Explain the reverse biasing of p-n junction diode.

Ans. : • When an external d.c. voltage is connected in such a way that p region is connected to negative and n region to positive terminal of the d.c. voltage then the biasing is called **reverse biasing**. It is shown in the fig. Q.5.1.



(a) Reverse biasing

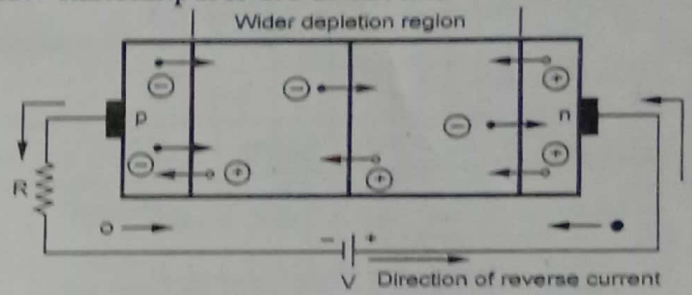


(b) Symbolic representation

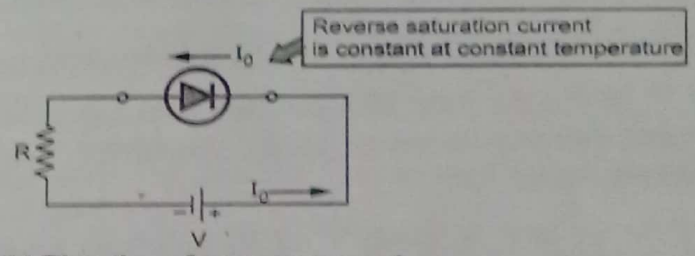
Fig. Q.5.1

- In reverse biasing, negative of battery attracts the holes in p region and positive of battery attracts the electrons in n region away from the junction.
- This widens the depletion region and barrier potential increases. No majority charge carrier can cross the junction.
- The resistance of the reverse biased diode is very high and the diode is said to be nonoperative in the reverse biased.

- However due to increased barrier potential, the free electrons on p side are dragged towards positive while holes on n side are dragged towards negative of the battery.
- This constitutes a current called **reverse current**. It flows due to **minority charge carriers** and hence its magnitude is very very small.
- For constant temperature, the reverse current is almost constant though applied reverse voltage is increased upto certain limit. Hence it is called **reverse saturation current** denoted as I_0. This is shown in the Fig. Q.5.2.
- The reverse current I_0 is of the order of few microamperes for Ge and few nanoamperes for Si diodes.



(a) Flow of minority charge carriers



(b) Direction of reverse current

Fig. Q.5.2 Reverse biased diode

1.6 : V-I Characteristics of Diode

Q.6 Draw and explain V-I characteristics of a p-n junction diode.

Ans. : • The graph of voltage applied across the p-n junction and the current flowing through the p-n junction is called **V-I characteristics** of p-n junction.

Forward Characteristics :

- In forward biasing V_f is the voltage across the p-n junction and I_f is the forward current hence graph of I_f against V_f is called forward characteristics of p-n junction.
- The forward characteristics of a diode is shown in the Fig. Q.6.1.

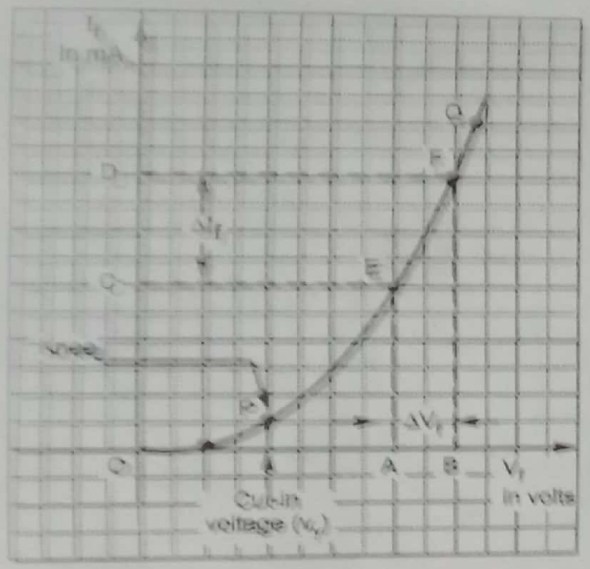


Fig. Q.6.1 Forward characteristics of a diode

- Basically forward characteristics can be divided into two regions :

1. **Region O to P :** As long as V_f is less than cut-in voltage (V_γ), the current flowing is very small. Practically this current is assumed to be zero.
2. **Region P to Q and onwards :** As V_f increases towards V_γ the width of depletion region goes on reducing. When V_f exceeds V_γ i.e. cut-in voltage, the depletion region becomes very thin and current I_f increases suddenly. This increase in the current is **exponential** as shown in the Fig. Q.6.1 by the region P to Q.

- The point P, after which the forward current starts increasing exponentially is called **knee** of the curve.

- The forward current is the conventional current, hence it is treated as positive and the forward voltage V_f is also treated positive. Hence the forward characteristics is plotted in the first **quadrant**.

Reverse Characteristics :

- The reverse voltage across the diode is V_R and reverse current through the diode is I_R hence graph of I_R against V_R is called reverse V-I characteristics of p-n junction.
- The polarity of V_R is opposite to V_f and direction of I_R is opposite to I_f hence both V_R and I_R are treated negative. Hence reverse characteristics are plotted in the **third quadrant**.
- As the reverse voltage is increased, reverse current increases initially but after a small voltage becomes constant equal to reverse saturation current I_0. This point is shown as P, in the Fig. Q.6.2.
- After this, though reverse voltage is increased, the reverse current remains constant till point A.
- At point A, reverse breakdown of the diode occurs and current increases sharply damaging the diode. This point is called knee of the reverse characteristics.
- The voltage corresponding to point A is called **reverse breakdown voltage** of the p-n junction denoted as V_{BR}.
- The reverse characteristics is shown in the Fig. Q.6.2.

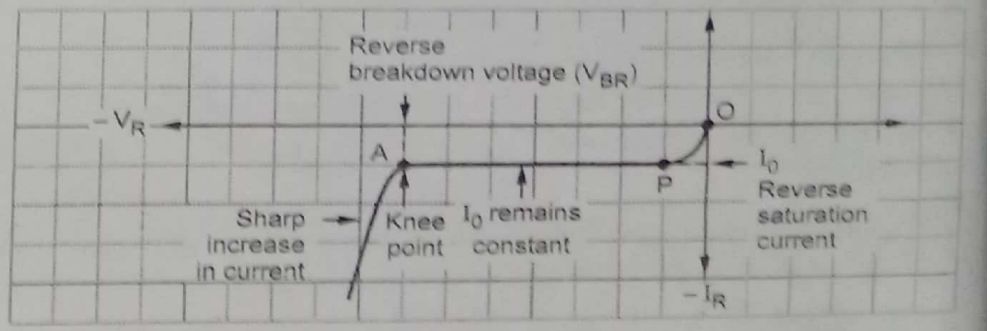


Fig. Q.6.2 Reverse characteristics of p-n junction diode

Q.7 Draw and comment on the V-I characteristics of typical Ge and Si diodes.

Ans. : • The cut-in voltage for germanium (Ge) diode is about 0.2 V while for Silicon (Si) diode is as about 0.6 V.

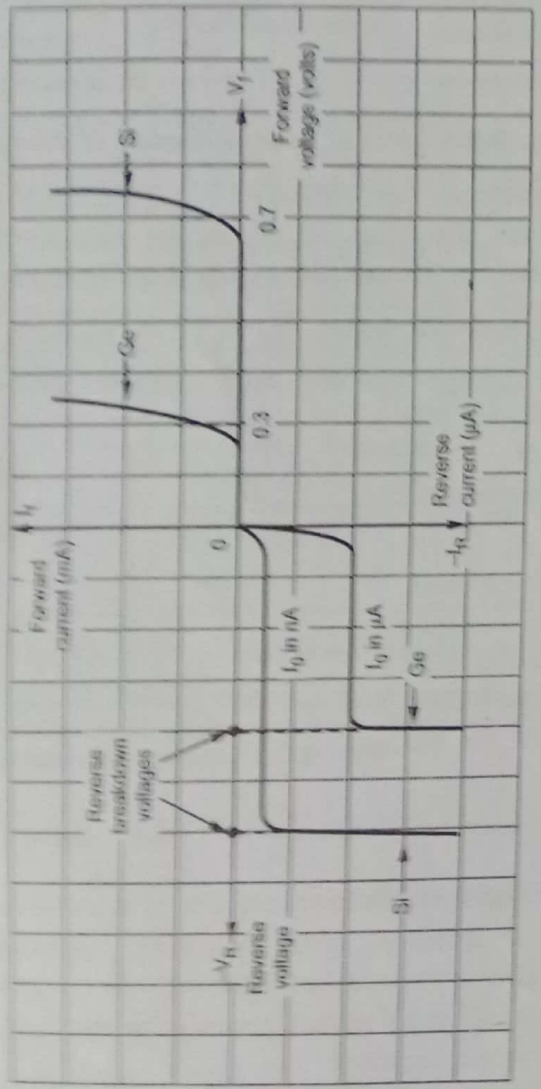


Fig. Q.7.1 V-I characteristics of typical Ge and Si diodes

- The potential at which current starts increasing exponentially is also called **offset potential, threshold potential** or **firing potential** of a diode.
- The Fig. Q.7.1 shows the V-I characteristics of typical Ge and Si diodes.
- The reverse saturation current I_0 is of the order of nA for silicon diode while it is of the order of μA for germanium diode.
- Reverse breakdown voltage for Si diode is higher than that of the Ge diode of a comparable rating.

1.7 : Ideal Diode

Q.8 Compare ideal and practical diode.

Ans. :

Sr. No.	Ideal diode	Practical diode
1.	The cut-in voltage is zero.	It has finite but small cut-in voltage.
2.	The internal forward resistance is zero.	It has small finite internal forward resistance.
3.	The voltage drop across forward biased ideal diode is zero.	There is finite voltage drop across forward biased practical diode.
4.	It acts as a short circuit (closed switch) in forward biased condition.	It does not act as a short circuit in forward biased condition.
5.	The internal resistance is infinite in reverse biased condition.	The internal resistance is very high but finite in reverse biased condition.
6.	It acts as on open circuit (open switch) in reverse biased condition.	It does not act as an open circuit in reverse biased condition. It carries very small reverse current.
7.	It does not exist in practice.	All the diodes are practical diodes.

Important Points To Remember

- Characteristics of ideal diode are shown in the Fig. 1.1.

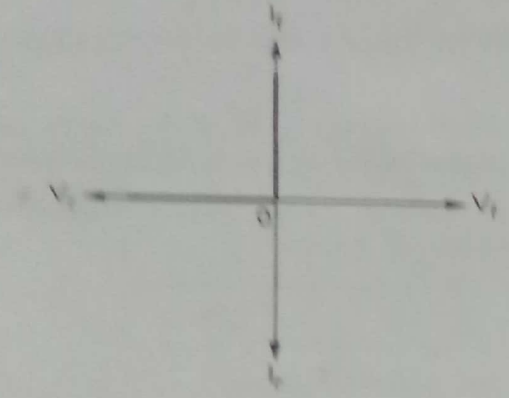


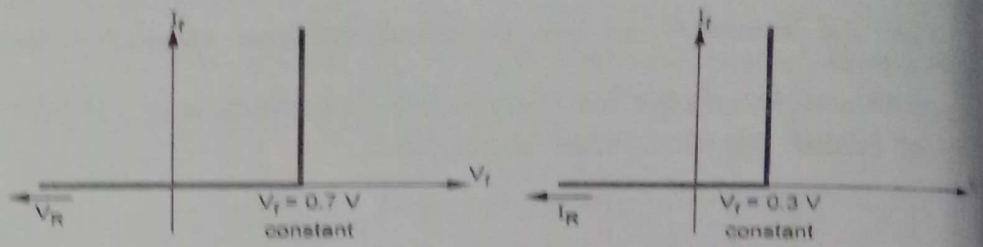
Fig. 1.1

- It can be seen that cut-in voltage is zero and diode conducts immediately when forward biased.
- In reverse biased, the reverse current is zero so it acts as an open switch.

1.8 : Second and Third Approximation

Q.9 Explain the second and third approximations of diode.

Ans. : Second approximation of diode : Practically the dynamic resistance of a diode is very small and is neglected. Due to this, the diode forward voltage drop is assumed constant equal to cut-in voltage of the diode. Thus the forward voltage drop of silicon diode is assumed constant equal to its cut-in voltage of 0.7 V while that of germanium diode is of 0.3 V. The reverse current is very small and neglected hence the diode is assumed to be open circuit in reverse biased condition. The second approximation characteristics is shown in the Fig. Q.9.1.



(a) Silicon diode (b) Germanium diode

Fig. Q.9.1 Second approximation of diode

Third approximation of diode : The approximation of characteristics with the help of pieces of straight lines is called third approximation or **linear piecewise approximation**.

- To obtain this approximation, $V_f = V_T = V_\gamma$ (cut in voltage) is marked on the voltage axis and then a straight line is drawn with a slope equal to the reciprocal of the dynamic resistance (r_d) of the diode.
- Thus the approximation consists of two straight lines, one horizontal and other with slope ($1/r_d$) as shown in the Fig. Q.9.2.

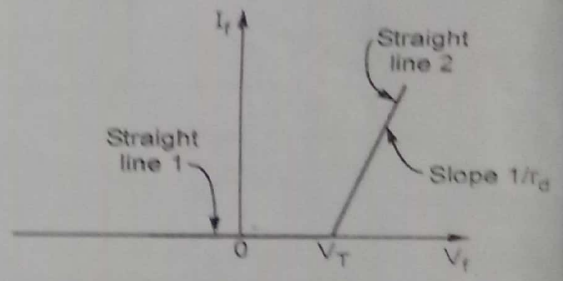


Fig. Q.9.2 Linear piecewise approximation

Q.10 Give the equivalent circuits of diode based on various approximations.

Ans. : For the analysis of various circuits, it is necessary to replace the diode by a battery and resistance depending on the approximation. This circuit is called equivalent circuit or circuit model of diode. In all such circuit models the reverse biased diode is assumed to be open circuited.

The Table Q.10.1 gives the equivalent circuits of a diode based on various approximations.

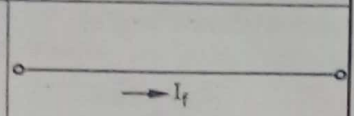
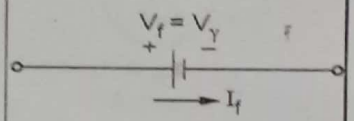
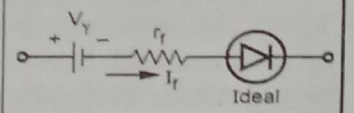
Sr. No.	Diode approximation	Behaviour	D.C. Equivalent circuit
1.	Ideal diode	$R_f = 0\ \Omega$ $R_r = \infty\ \Omega$ Short in forward bias.	
2.	Diode with constant forward voltage drop	The forward voltage drop is constant and it behaves as d.c. battery of voltage $V_f = V_\gamma$	
3.	Complete d.c. equivalent circuit	This assumes finite forward resistance which is its dynamic forward resistance r_f in series with battery of voltage V_γ.	 Ideal Total diode drop is, $V_f = V_\gamma + I_f r_f$

Table Q.10.1 D.C. Equivalent circuits of diode

Q.11 For the circuit shown, find the load voltage, load current and diode power using third approximation. Assume silicon diode with resistance of 0.2 Ω.

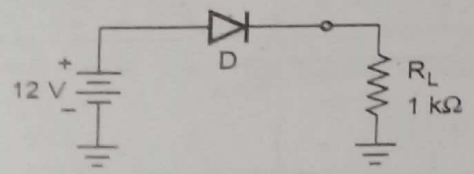


Fig. Q.11.1

Ans. : Replace diode by its equivalent circuit according to third approximation as shown in the Fig. Q.11.1(a).

Applying KVL,

$-0.7 - 0.2\ I_f - 1000\ I_f + 12 = 0$ i.e.

$I_f = \mathbf{11.297\ mA}$

$V_f = 0.7 + I_f r_f$

$= 0.7 + 11.297 \times 10^{-3} \times 02$

$= 0.70225$ V

$V_L = 11.297 \times 10^{-3} \times 1 \times 10^3$

$= \mathbf{11.297\ V}$

$P_D = V_f I_f = 0.70225 \times 11297 \times 10^{-3} = \mathbf{7.933\ mW}$

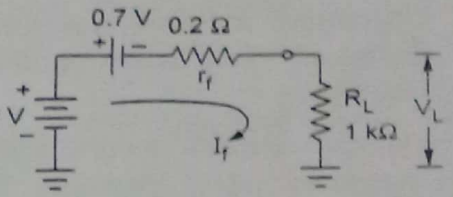


Fig. Q.11.1 (a)

1.9 : Surface Mount Diodes

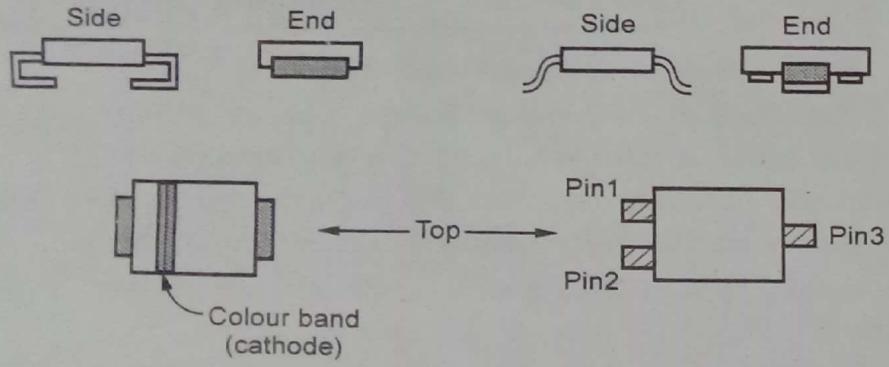
Q.12 Write a note on surface mount diodes.

Ans. : The diodes which can be mounted on the surface of a circuit board are called surface mounting diodes. These diodes are easy to test and can be easily removed and replaced on the circuit board. These diodes are relatively small and efficient in operation.

- The surface mount (SM) is one of the package styles used in the industry.
- The surface mount package uses two L bend leads and a coloured band on one end of the body which indicates the cathode lead.
- The Fig. Q.12.1(a) shows the two terminal surface mount style package used for the surface mount diodes.
- The total dimensions of such a surface mount style package depends on the current rating of the diode. The surface area is larger for high current rating diodes.
- In the high current rating diodes the heat produced at the junction is more which is to be dissipated as quickly as possible

Increased surface area helps to increase the ability of the diode to dissipate the heat generated to keep the temperature within the specified limits.

- Increasing the width of the mounting terminals produces the effect of virtual heat sink, increasing the thermal conductance of the diode.
- Another surface mount style package is called small outline transistor (SOT) package. This package includes two diodes having common anode or common cathode connection as one of the terminals. These packages are small and used for the diodes with current rating less than 1 ampere. Due to small size it is difficult to provide the identification codes for such diodes.
- The Fig. Q.12.1(b) shows SOT style package.



(a) SM style packge (b) SOT style package

Fig. Q.12.1

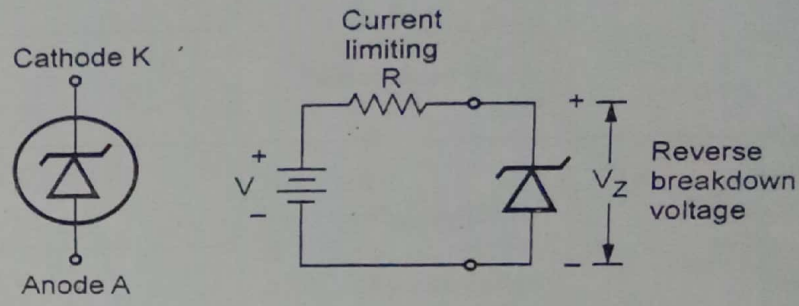
1.10 : Zener Diode

Q.13 What is zener diode ? Explain its V-I characteristics.

Ans. : • A zener diode is a silicon p-n junction semiconductor device which is operated in its **reverse breakdown** region.

- The zener diodes are fabricated with precise breakdown voltages by controlling the doping level during manufacturing.

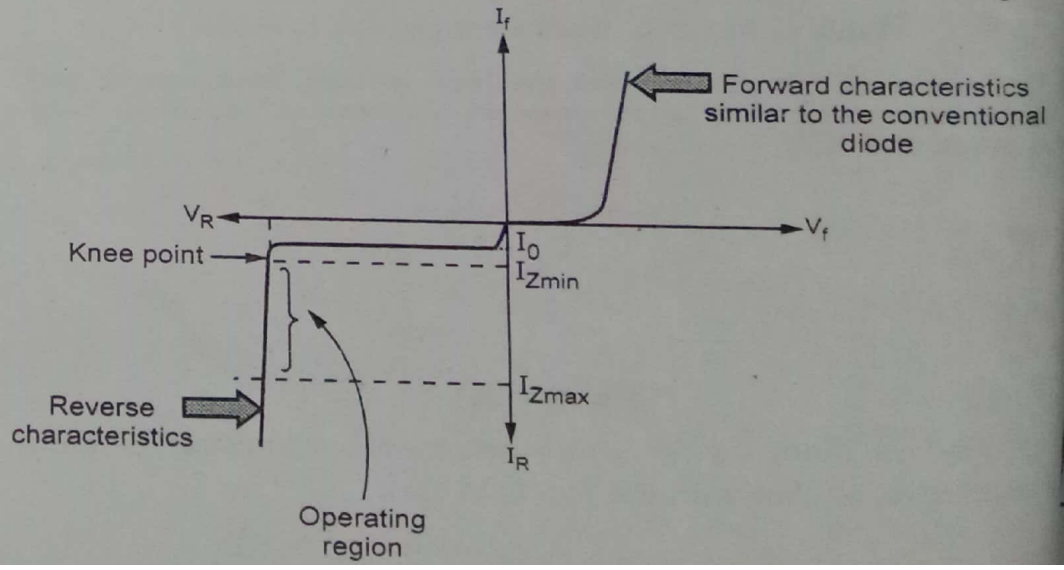
- The Fig. Q.13.1 (a) shows the symbol of zener diode while the Fig. Q.13.1 (b) shows the the operation of zener diode in reverse breakdown region.



(a) Symbol (b) Reverse biasing

Fig. Q.13.1 Zener diode

- When the reverse voltage is applied to zener diode, at a certain reverse voltage, the reverse breakdown occurs and current in the zener diode increases rapidly. The sharp change in the zener current is called **knee** or **zener knee** of the reverse characteristics.
- The reverse bias voltage at which the breakdown occurs is called **zener breakdown voltage**, denoted as V_Z. This value is carefully designed by controlling the doping level during manufacturing.



- The V-I characteristics of zener diode is shown in the Fig. Q.13.2.
- For zener diodes, practically two currents are specified. The I_{Zmin} is minimum current through the zener diode to maintain its reverse breakdown operation.
- The I_{Zmax} is the maximum current which zener diode can take safely maintaining its reverse breakdown operation, i.e. constant V_Z across it.

Q.14 Compare between zener and avalanche breakdown.

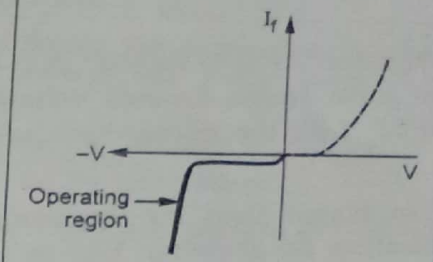
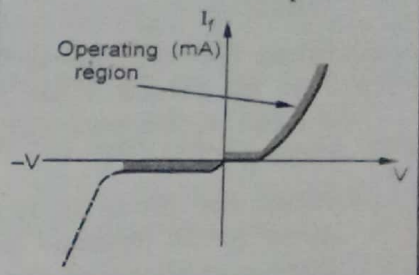
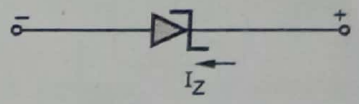
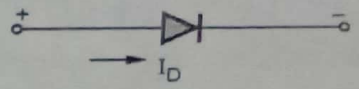
Ans. :

Sr. No.	Zener breakdown	Avalanche breakdown
1.	Breakdown is due to intense electric field across the junction.	Breakdown is due to the collision of accelerated charge carriers with the adjacent atoms and due to carrier multiplication.
2.	Occurs for zeners with zener voltage less than 6 V.	Occurs for zeners with zener voltage greater than 6 V.
3.	The temperature coefficient is negative.	The temperature coefficient is positive.
4.	The breakdown voltage decreases as junction temperature increases.	The breakdown voltage increases as junction temperature increases.
5.	The V-I characteristics is very sharp in breakdown region.	The V-I characteristics is not as sharp as zener breakdown.

Q.15 Compare zener diode and the conventional p-n junction diode.

Ans. :

No.	Zener diode	P-N junction diode
1.	Operated in reverse breakdown condition.	Operated in forward biased condition and never operated in reverse breakdown condition.

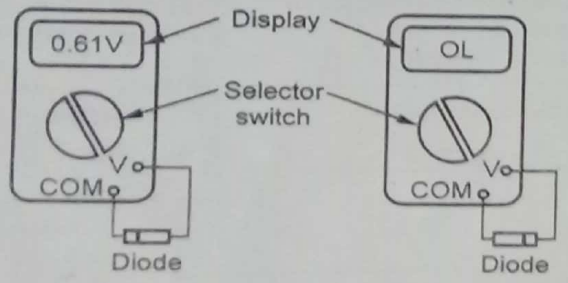
2.	The important region of operation lies in third quadrant. 	The important region of operation lies in first quadrant. 
3.	Dynamic zener resistance is very small in reverse breakdown condition.	The diode resistance in reverse biased condition is very high.
4.	Zener diode symbol is, 	The p-n junction diode symbol is, 
5.	The conduction in zener is opposite to that of arrow in the symbol, as operated in breakdown region.	The conduction when forward biased is in same direction as that of arrow in the symbol, when forward biased.
6.	The power dissipation capability is very high.	The power dissipation capability is very low compared to zener diodes.
7.	Applications of zener diode are voltage regulator, protection circuits, voltage limiters etc.	Applications of p-n junction diode are rectifiers, voltage multipliers, clippers, clampers and many electronic devices.

1.11 : Testing of Diode with Multimeter

Q.16 Explain the testing of diode with multimeter.

Ans. : • Digital multimeter has the diode testing ternimals or special diode test range.

- When the multimeter is used on this test range then it supplies a constant current of about 1 mA to a diode connected to its terminals.
- When the terminals are connected so as to forward bias the diode then for perfect diode, the meter shows forward voltage drop of the diode. It shows 0.55 to 0.7 V for the silicon diode as shown in the Fig. Q.16.1 (a).
- When the diode is reverse biased then for the perfect diode, meter gives overload indication by showing 'OL' or '1' on the display as shown in the Fig. Q.16.1 (b).



(a) Forward biased (b) Reverse biased

Fig. Q.16.1 Testing of diode with multimeter

- If 'OL' display occurs for both forward and reverse bias connections then diode is open circuited.
- While if the display shows '000' in both forward and reverse biased cases then the diode is short circuited.

1.12 : Rectifier

Q.17 What is rectifier ? What are its types ?

Ans. : • A **rectifier** is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diodes.

- The three types of rectifiers using diodes are,
  - i) Half wave rectifier
  - ii) Full wave rectifier with center tap
  - iii) Bridge rectifier.

1.13 : Half Wave Rectifier

Q.18 Draw the half wave rectifier and explain its operation along with the waveforms.

Ans. : • The circuit diagram is shown in the Fig. Q.18.1.

- A sinusoidal a.c. voltage, having frequency of 50 Hz is applie to rectifier circuit using suitable step-down transformer, wit necessary turns ratio.

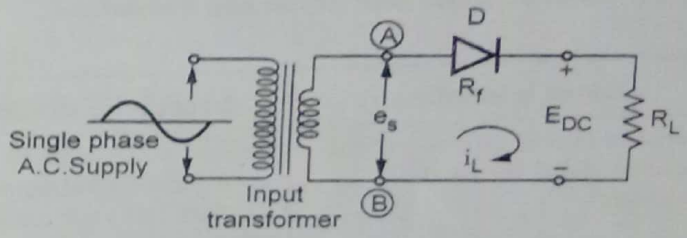


Fig. Q.18.1 Halfwave rectifier

- The transformer secondary voltage e_s is mathematically given by,

$$e_s = E_{sm} \sin \omega t$$

with $\omega = 2\pi f$ and

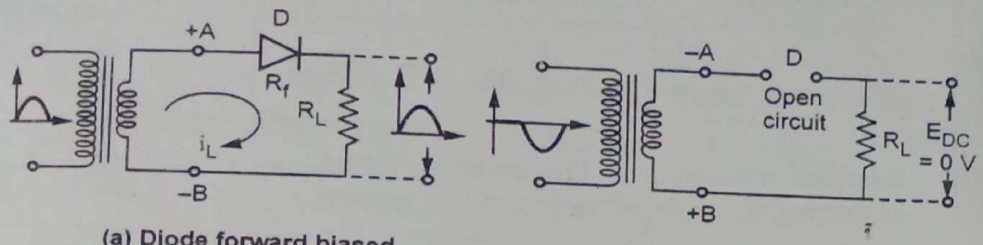
f = Supply frequency

- The turns ratio of transformer decides the secondary voltage e_s which is applied to rectifier.

Operation of the Circuit :

- During the positive half cycle of input a.c. voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in the Fig. Q.18.2 (a). This current is also flowing through the load resistance R_L hence denoted as i_L (load current).
- During negative half cycle when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Thus it acts

as an open circuit. Hence no current flows in the circuit as shown in the Fig. Q.18.2 (b).



(a) Diode forward biased (b) Diode reverse biased

Fig. Q.18.2

- Thus the circuit current, which is also the load current, is in the form of half sinusoidal pulses.
- The load voltage, being the product of load current and load resistance, will also be in the form of half sinusoidal pulses. The different waveforms are illustrated in Fig. Q.18.3.

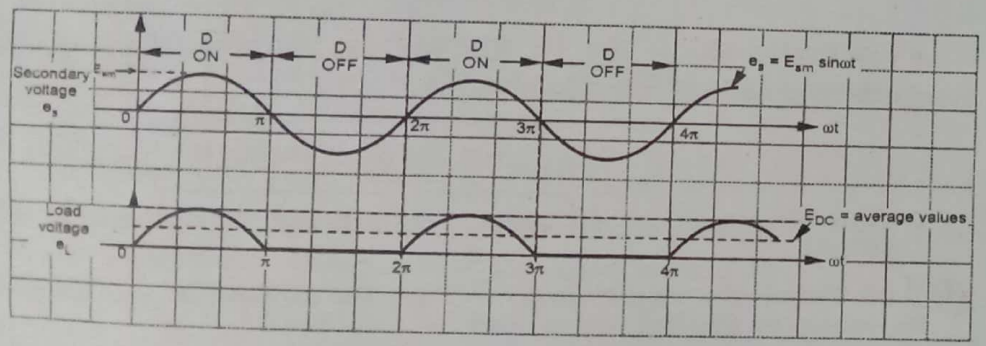


Fig. Q.18.3 Load current and load voltage waveforms for half wave rectifier

Important Points to Remember

- The peak value of the load current is given by,

$$\therefore \quad I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

where

R_s = Resistance of secondary winding of transformer

R_f = Forward resistance of diode

- If R_s and R_f are not given they should be neglected while calculating I_m.

Q.19 Derive the expression for the d.c. load current, average d.c. load voltage and r.m.s. value of load current for the half wave rectifier.

Ans. : • **The average or d.c. value of the load current (I_{DC})** : It is obtained by integration.

- Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \quad \text{for } 0 \le \omega t \le \pi$$

and $$i_L = 0 \quad \text{for } \pi \le \omega t \le 2\pi$$

where I_m = Peak value of load current

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

- As no current flows during negative half cycle of a.c. input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t) = \frac{I_m}{2\pi}[-\cos(\omega t)]_0^{\pi}$$

$$= -\frac{I_m}{2\pi}[\cos(\pi) - \cos(0)] = -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$$

$$\therefore \quad \boxed{I_{DC} = \frac{I_m}{\pi} = \text{Average value}}$$

The average d.c. load voltage (E_{DC}) : It is the product of average D.C. load current and the load resistance R_L.

$$\therefore \quad \boxed{E_{DC} = I_{DC} R_L = \frac{I_m}{\pi} R_L = \frac{E_{sm}}{(R_f + R_L + R_s)\pi} R_L}$$

- The winding resistance R_s and forward diode resistance R_f are practically very small compared to R_L hence neglecting them,

$$\therefore \quad E_{DC} \approx \frac{E_{sm}}{\pi}$$

The RMS value of the load current (I_{RMS}) :

- The RMS means squaring, finding mean and then square root. Mathematically it is obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(I_m \sin \omega t)^2 \, d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t \; d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\int_0^{\pi}\frac{1-\cos 2\omega t}{2} d(\omega t)} = I_m \sqrt{\frac{1}{2\pi}\left\{\frac{\omega t}{2} - \frac{\sin 2\omega t}{4}\right\}_0^{\pi}}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2}\right)} = \frac{I_m}{2} \qquad \ldots \sin(2\pi) = \sin(0) = 0$$

$$\therefore \quad I_{RMS} = \frac{I_m}{2} \text{ and } E_{L(RMS)} = I_{RMS} R_L = \frac{I_m}{2} R_L = \frac{E_{sm}}{2}$$

Q.20 Derive the expression for the efficiency of half wave rectifier. And show that maximum theoretical efficiency of a half wave rectifier is 40.6 %.

Ans. : • The **d.c. power output** is,

$$\therefore \quad P_{DC} = E_{DC} I_{DC} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi}\right]^2 R_L = \frac{I_m^2}{\pi^2} R_L$$

$$\therefore \quad P_{DC} = \frac{E_{sm}^2 R_L}{\pi^2 [R_f + R_L + R_s]^2} \quad \text{using } I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

- The **a.c. power input** taken from the secondary of transformer is the power supplied to three resistances namely load resistance R_L, the diode resistance R_f and winding resistance R_s.

The a.c. power is, $P_{AC} = I_{RMS}^2 [R_L + R_f + R_s]$ but $I_{RMS} = \frac{I_m}{2}$ for wave,

$$\therefore \quad P_{AC} = \frac{I_m^2}{4} [R_L + R_f + R_s]$$

Rectifier efficiency : The **rectifier efficiency** is defined as the of output d.c. power to input a.c. power.

$$\eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}} = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4}[R_f + R_L + R_s]} = \frac{(4/\pi^2) R_L}{(R_f + R_L + R_s)}$$

$\therefore$ Dividing by R_L to numerator and denominator,

$$\eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L}\right)}$$

- Practically $(R_f + R_s) \ll R_L$, we get the maximum theore efficiency of half wave rectifier as,

$$\therefore \quad \%\, \eta_{max} = 0.406 \times 100 = 40.6\ \%$$

- **More the rectifier efficiency, less are the ripple contents i output.**

Q.21 Define the ripple factor. Derive its expression and hence its value for the half wave rectifier.

Ans. : • The measure of ripples present in the output is wit help of a factor called **ripple factor** denoted by γ. It tells smooth is the output.

- Mathematically **ripple factor** is defined as the ratio of R.M.S. of the a.c. component in the output to the average or component present in the output.

$$\therefore \quad \text{Ripple factor } \gamma = \frac{\text{R.M.S. value of a.c. component of out}}{\text{Average or d.c. component of output}}$$

- The output current is composed of a.c. component as well as d.c. component.

Let I_{ac} = R.M.S. value of a.c. component present in output

I_{DC} = D.C. component present in output

- I_{RMS} = R.M.S. value of total output current = $\sqrt{I_{ac}^2 + I_{DC}^2}$

i.e. $I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$

$$\text{Ripple factor} = \frac{I_{ac}}{I_{DC}} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$ ... As per definition

- For a half wave circuit, $I_{RMS} = \frac{I_m}{2}$ while $I_{DC} = \frac{I_m}{\pi}$

- Using in the above expression for the ripple factor,

$$\gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2}\right)}{\left(\frac{I_m}{\pi}\right)}\right]^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674} = \mathbf{1.21}$$ ... Halfwave

This indicates that the ripple contents in the output are 1.21 times the d.c. component i.e. 121.1 % of d.c. component.

Important Points To Remember

- The voltage regulation is the factor which tells us about the change in the d.c. output voltage as load changes from no load to full load condition.
- If $(V_{dc})_{NL}$ = D.C. voltage on no load and $(V_{dc})_{FL}$ = D.C. voltage on full load then voltage regulation is defined as,

$$\% \text{ Voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

- **Less the value of voltage regulation, better is the performance of rectifier circuit.**

Transformer Utilization Factor (TUF)

- The T.U.F. is defined as the ratio of d.c. power delivered to the load to the a.c. power rating of the transformer.

$$\therefore \text{T.U.F.} = \frac{\text{D.C. power delivered to the load}}{\text{A.C. power rating of the transformer}} = \mathbf{0.287} \text{ for half wave.}$$

Q.22 A half wave rectifier from supply 230 V 50 Hz with step down transformer ratio 3 : 1 to a resistive load of 10 $k\,\Omega$. The diode forward resistance is 75 Ω and transformer secondary is 10 Ω. Calculate the DC current, DC voltage, efficiency and ripple factor.

Ans. : $R_L = 10\ k\Omega,\ R_f = 75\ \Omega,\ R_s = 10\ \Omega$

$E_{P(RMS)} = 230\ V,\ N_2/N_1 = 1 : 3$

$$\frac{N_2}{N_1} = \frac{E_{s\,(RMS)}}{E_{p\,(RMS)}} \quad \text{i.e.} \quad \frac{1}{3} = \frac{E_{s\,(RMS)}}{230}$$

$\therefore E_{s\,(RMS)} = 76.667\ V$

$\therefore E_{sm} = \sqrt{2} \times E_{s\,(RMS)} = 108.423\ V$

$$\therefore I_m = \frac{E_{sm}}{R_L + R_f + R_s} = 10.751\ mA$$

$$\therefore I_{DC} = \frac{I_m}{\pi} = \mathbf{3.422\ mA}$$

$$\therefore E_{DC} = I_{DC} R_L = 3.422 \times 10^{-3} \times 10 \times 10^3$$

$$= \mathbf{34.22\ V}$$

$$I_{RMS} = \frac{I_m}{2} = 5.3755\ mA$$

$\therefore P_{DC} = E_{DC} I_{DC} = 0.1171\ W$

$\therefore P_{AC} = I_{RMS}^2 (R_L + R_s + R_f) = 0.2914\ W$

$$\% \eta = \frac{P_{DC}}{P_{AC}} \times 100 = 40.18\ \%$$

$$\text{Ripple factor} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = 1.21$$

1.14 : Full Wave Rectifier

Q.23 With the help of circuit diagram and waveforms, explain the working of centre-tap full wave rectifier.

Ans. : • The full wave rectifier circuit is shown in the Fig. Q.23.1.

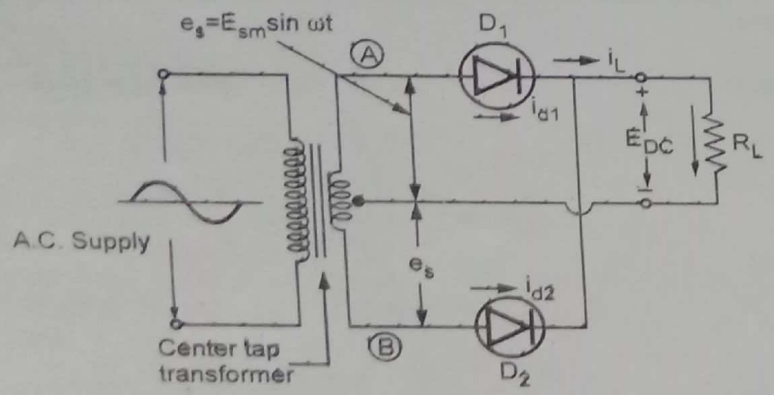


Fig. Q.23.1 Full wave rectifier

- It uses a center tap transformer.
- It uses two diodes which feed a common load resistance R_L.
- The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

Operation of the Circuit :

- Consider the positive half cycle of ac input voltage in which terminal (A) is positive and terminal (B) is negative due to center tap transformer.

- The diode D_1 will be forward biased and hence will cond while diode D_2 will be reverse biased and will act as an op circuit and will not conduct. The diode D_1 supplies the lo current, i.e. $i_L = i_{d1}$.
- In the next half cycle of ac voltage, polarity reverses and termi (A) becomes negative and (B) positive. The diode D_2 condu being forward biased, while D_1 does not, being reverse biase The diode D_2 supplies the load current, i.e. $i_L = i_{d2}$.
- The **load current flows in both the half cycles of ac voltage a in the same direction through the load resistance**. Hence we g rectified output across the load.
- The load current is sum of individual diode currents flowing corresponding half cycles.
- The waveforms of secondary voltage (one half), load current a load voltage are shown in the Fig. Q.23.2.

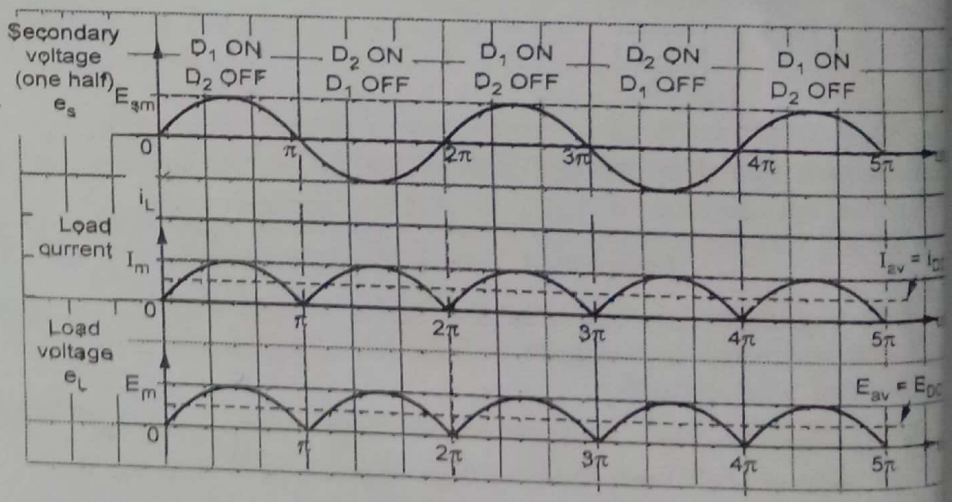


Fig. Q.23.2 Load current and voltage waveforms for full wave rectif

Important Points to Remember

- R_f = Forward resistance of diodes and R_L = Load resistance
- R_s = Winding resistance of **each half** of secondary
- E_{sm} = Maximum value of a.c. input voltage across **each half** of secondary winding
- The maximum value of the load current $I_m = \frac{E_{sm}}{R_s + R_f + R_L}$.

Q.24 Derive the expressions for the average d.c. current, d.c. load voltage and RMS value of the load current for the full wave rectifier circuit with two diodes.

Ans. : The average or d.c. value of the load current (I_{DC}) :

- Consider one cycle of the load current i_L from 0 to π to obtain the average value which is d.c. value of load current.

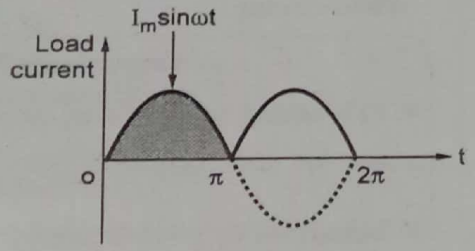


Fig. Q.24.1 Load current waveform

$$i_L = I_m \sin \omega t \qquad 0 \le \omega t \le \pi$$

$$I_{av} = I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t)$$

$$= \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t \, d\omega t$$

$$= \frac{I_m}{\pi}\left[(-\cos \omega t)_0^{\pi}\right] = \frac{I_m}{\pi}\left[-\cos \pi - (-\cos 0)\right]$$

$$= \frac{I_m}{\pi}\left[+1 - (-1)\right] \qquad \ldots \cos \pi = -1$$

$$\therefore \boxed{I_{DC} = \frac{2I_m}{\pi}}$$

Average DC Load Voltage (E_{DC}) :

- The d.c. load voltage is, $E_{DC} = I_{DC} R_L = \frac{2I_m R_L}{\pi}$

Substituting value of I_m,

$$E_{DC} = \frac{2E_{sm} R_L}{\pi\left[R_f + R_s + R_L\right]} = \frac{2E_{sm}}{\pi\left[1 + \frac{R_f + R_s}{R_L}\right]}$$

- But as R_f and $R_s \ll R_L$ hence $\frac{R_f + R_s}{R_L} \ll 1$,

$$\therefore \boxed{E_{DC} = \frac{2E_{sm}}{\pi}}$$

RMS Load Current (I_{RMS}) : Mathematically it can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)} = \sqrt{2 \times \frac{1}{2\pi}\int_0^{\pi} [I_m \sin(\omega t)]^2 \, d(\omega t)}$$

- The circuit has two half wave rectifiers similar in operation operating in two half cycles hence integration term is splitted as above.

$$\therefore I_{RMS} = I_m \sqrt{\frac{1}{\pi}\int_0^{\pi} \sin^2(\omega t) d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{1 - \cos 2\omega t}{2} \, d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\left[\frac{\omega t}{2} - \frac{\sin(2\omega t)}{4}\right]_0^{\pi}} = I_m \sqrt{\frac{1}{\pi}\left[\frac{\pi}{2}\right]}$$

$$\therefore \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}} \text{ and } E_{L(RMS)} = I_{RMS} R_L = \frac{I_m}{\sqrt{2}} R_L}$$

Q.25 For a full wave rectifier with two diodes, prove that its ripple factor is 0.48 and its maximum efficiency is 81.2 %.

Ans. : Maximum theoratical efficiency :

- D.C. Power output = $E_{DC} I_{DC} = I_{DC}^2 R_L$

$$\therefore \quad P_{DC} = \left(\frac{2I_m}{\pi}\right)^2 R_L = \frac{4}{\pi^2} \frac{E_{sm}^2}{(R_s + R_f + R_L)^2} \times R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$\therefore \quad \text{AC power input } P_{AC} = I_{RMS}^2 (R_f + R_s + R_L)$$

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$= \frac{I_m^2 (R_f + R_s + R_L)}{2}$$

- Substituting value of I_m we get,

$$\therefore \quad P_{AC} = \frac{E_{sm}^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L) = \frac{E_{sm}^2}{2(R_f + R_s + R_L)}$$

$$\therefore \quad \text{Rectifier efficiency } \eta = \frac{P_{DC} \text{ output}}{P_{AC} \text{ input}} = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}}$$

$$= \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

- But if $R_f + R_s \ll R_L$, neglecting it from denominator,

$$\eta_{max} = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2}$$

$$\therefore \quad \% \eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2 \%$$

Ripple factor :

- The ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

- For full wave $I_{RMS} = I_m / \sqrt{2}$ and $I_{DC} = 2I_m / \pi$ so substitutin above,

$$\therefore \quad \text{Ripple factor} = \gamma = \sqrt{\left[\frac{I_m / \sqrt{2}}{2I_m / \pi}\right]^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

- This indicates that the ripple contents in the output are 48 % the d.c. component which is much less than that for the ha wave circuit.

Important Points to Remember

- **PIV rating of diode in two diode full wave rectifier :**

  PIV of diode = 2 E_{sm}

- Note that E_{sm} = Maximum value of a.c. voltage across half th secondary of transformer.
- **The ripple frequency in full wave rectifier is '2f" Hz.**
- The average **TUF** for full wave rectifier is **0.693.**

Q.26 A single phase full-wave rectifier supplies power to a 1 k load. The AC voltage applied to the diode is 300-0-300 V. If diod resistance is 25 Ω and that of the transformer secondary negligible Determine average load current, average load voltage an rectification efficiency.

Ans. : Transformer voltage is 300 - 0 - 300 V

$$\therefore \quad E_{s\,(RMS)} = 300 \text{ V}, \quad E_{sm} = \sqrt{2} \times 300 = 424.264 \text{ V}$$

$$I_m = \frac{E_{sm}}{R_f + R_L} = \frac{424.264}{25 + 1 \times 10^3} = 0.4139 \text{ A}$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2\times0.4139}{\pi} = \mathbf{0.2635\ A}$$

$$E_{DC} = I_{DC}\ R_L = 0.2635\times 1\times 10^3$$

$$= \mathbf{263.5\ V}$$

$$P_{DC} = I_{DC}^2 R_L = 69.4322\ W,$$

$$P_{AC} = I_{RMS}^2 (R_f + R_L)$$

$$\therefore\quad P_{AC} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L) = 87.798\ W$$

$$\therefore\quad \%\ \eta = \frac{P_{DC}}{P_{AC}}\times 100 = \frac{69.4322}{87.798}\times 100$$

$$= \mathbf{79.081\ \%.}$$

1.15 : Bridge Rectifier

Q.27 Draw the circuit of bridge rectifier and explain its operation. Give the input and output waveforms.

Ans. : • The basic bridge rectifier circuit is shown in Fig. Q.27.1.

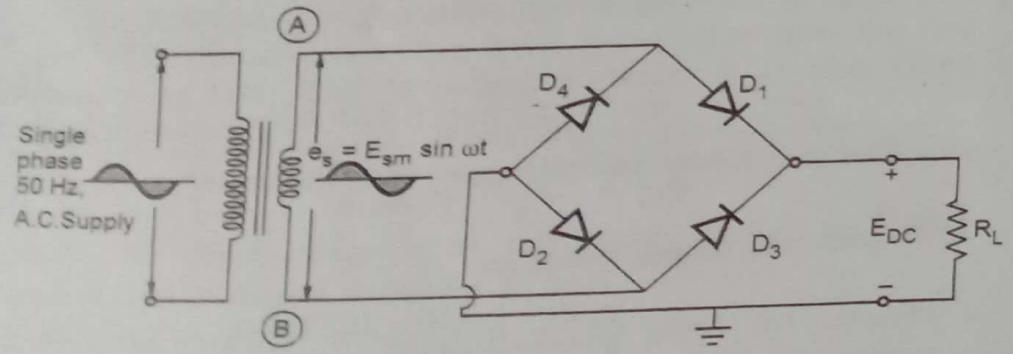


Fig. Q.27.1 Bridge rectifier circuit

• The bridge rectifier circuit is essentially a **full-wave rectifier** circuit, using four diodes, forming the four arms of an electrical bridge.

• To one diagonal of the bridge, the ac voltage is applied through a transformer if necessary and the rectified dc voltage is taken from the other diagonal of the bridge.

Operation of the circuit :

• Consider the positive half of ac input voltage. The point A of secondary becomes positive. The diodes D_1 and D_2 will be forward biased, while D_3 and D_4 reverse biased. The two diodes D_1 and D_2 conduct in series with the load and the current flows as shown in Fig. Q.27.2.

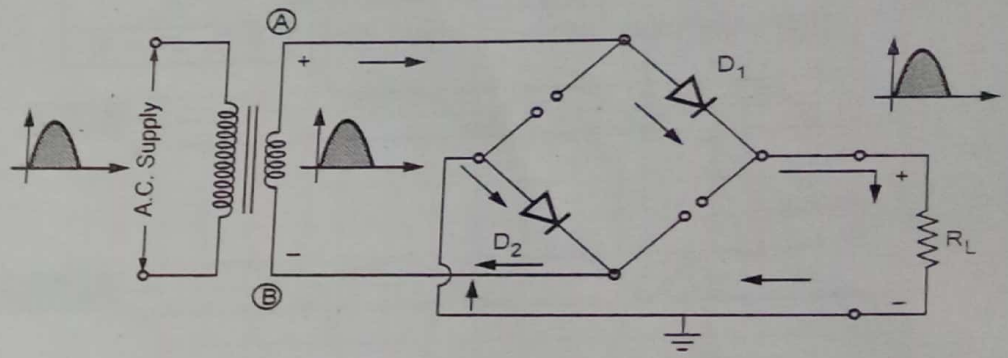


Fig. Q.27.2 Current flow during positive half cycle

• In the next half cycle, when the polarity of ac voltage reverses hence point B becomes positive diodes D_3 and D_4 are forward biased, while D_1 and D_2 reverse biased. Now the diodes D_3 and D_4 conduct is series with the load and the current flows as shown in Fig. Q.27.3.

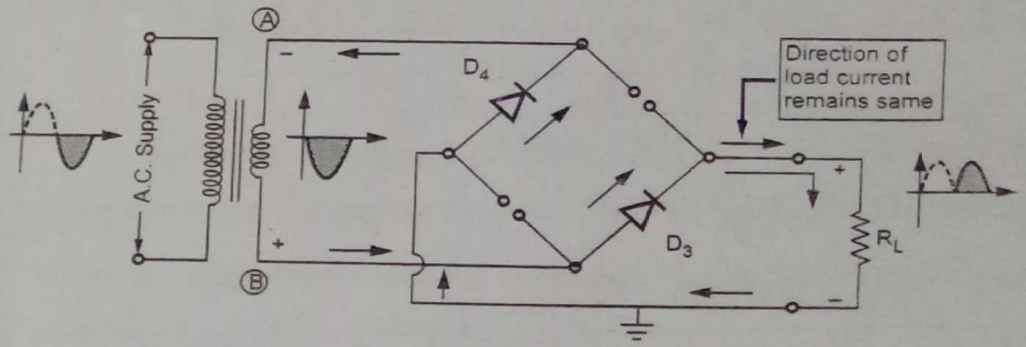


Fig. Q.27.3 Current flow during negative half cycle

- It is seen that in both cycles of ac, the load current is flowing in the same direction hence, we get a full-wave rectified output.
- The waveforms of load current and voltage are shown in the Fig. Q.27.4.

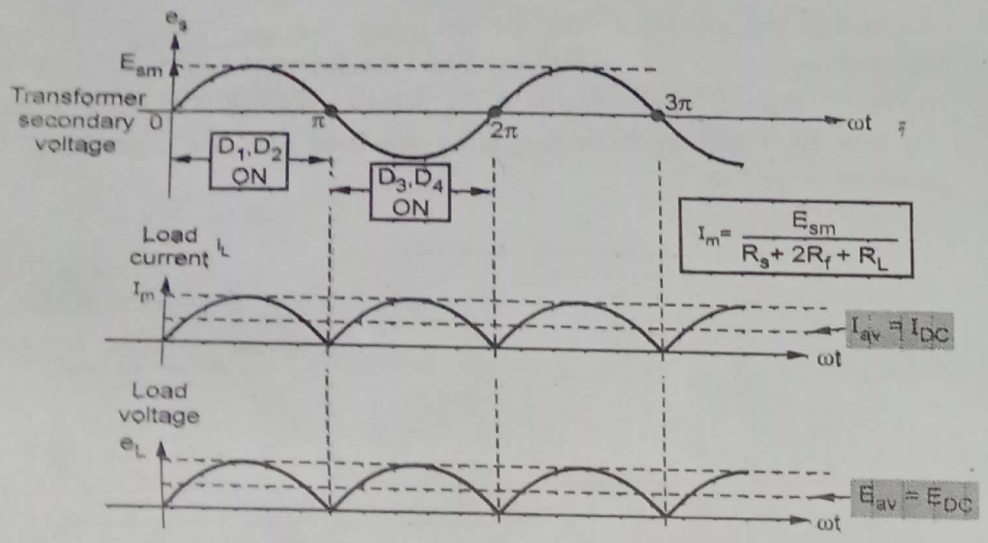


Fig. Q.27.4 Waveforms of bridge rectifier

Important Points to Remember

- **For bridge rectifier,** in each half cycle two diodes conduct hence in the various expressions R_f must be replaced by $2R_f$.
- $I_m = \dfrac{E_{sm}}{R_s + 2R_f + R_L}$
- $E_{DC} = I_{DC} R_L = \dfrac{2E_{sm}}{\pi}$,

  $E_{RMS} = \dfrac{I_m}{\sqrt{2}} R_L = \dfrac{E_{sm}}{\sqrt{2}(R_s + 2R_f + R_L)} R_L$
- $P_{DC} = I_{DC}^2 R_L = \dfrac{4}{\pi^2} I_m^2 R_L$ and

  $P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L)$

$$= \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

- $\eta = \dfrac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}$, $\%\ \eta_{max} = 81.2\ \%$,

  ripple factor $\gamma = 0.48$, T.U.F. $= 0.812$
- The E_{sm} is the maximum value of a.c. voltage across full secondary winding of the transformer used.
- PIV rating for the diodes used in bridge rectifier is E_{sm}.

Q.28 A bridge rectifier is driving a load resistance of 100 Ω. It is driven by a source voltage of 230 V, 50 Hz. Neglecting diode resistances, calculate : i) Average d.c. voltage ii) Average direct current iii) Frequency of output waveform.

Ans. : Given, $R_L = 100\ \Omega$, $E_{s\,(RMS)} = 230$ V, $R_f = 0$, $f = 50$ Hz

$$E_{sm} = \sqrt{2} \times E_{s(RMS)} = \sqrt{2} \times 230 = 325 \text{ V}$$

i) Average d.c. voltage

$$E_{DC} = \frac{2E_{sm}}{\pi} = \frac{2 \times 325}{\pi} = \mathbf{206.9\ V}$$

... As $R_f = 0$

ii) Average direct current

$$I_{DC} = \frac{2I_m}{\pi} \text{ where } I_m = \frac{E_{sm}}{R_L + 2R_f + R_s}$$

$$I_m = \frac{3.25}{100 + 0 + 0} = 3.25 \text{ A}$$

$$I_{DC} = \frac{2 \times 3.25}{\pi} = \mathbf{2.06\ A}$$

iii) Frequency of output waveform

$$= 2f = 2 \times 50 = \mathbf{100\ Hz}$$

1.16 : Filter

Q.29 Explain the need of the filter.

Ans. : • The output of a rectifier circuit is not pure d.c.; but it contains fluctuations or ripples, which are undesired.

It is seen that in both cycles of ac, the load current is flowing in the same direction hence, we get a full-wave rectified output.

The waveforms of load current and voltage are shown in the Fig. Q.27.x.

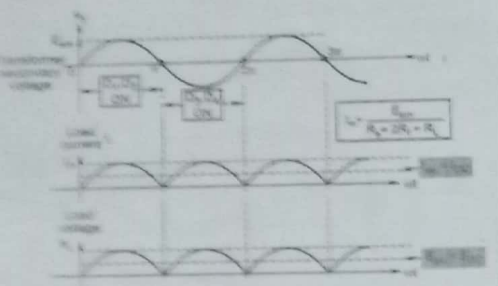


Fig. Q.27.x Waveforms of bridge rectifier

Important Points to Remember

- For bridge rectifier, in each half cycle two diodes conduct hence in the various expressions R_f must be replaced by $2R_f$.
- $I_m = \frac{E_{sm}}{R_L + 2R_f + R_s}$
- $I_{DC} = I_{AV} = \frac{2I_m}{\pi}$
- $V_{load} = I_{DC} R_L = \frac{2I_m}{\pi} R_L = \frac{2E_{sm}}{\pi(R_L + 2R_f + R_s)} R_L$
- $P_{DC} = \frac{V_{DC}}{I_{DC}} R_L = \frac{4}{\pi^2} I_{DC}^2 R_L$ and
- $\eta_{max} = \frac{81.2}{(1 + R_s/R_L + 2R_f/R_L)}$ %

$$= \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

- $\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}$ % $\eta_{max} = 81.2$ %,

  ripple factor $\gamma = 0.48$, T.U.F. = 0.812
- The E_{sm} is the maximum value of a.c. voltage across full secondary winding of the transformer used.
- PIV rating for the diodes used in bridge rectifier is E_{sm}.

Q.28 A bridge rectifier is driving a load resistance of 100 Ω. It is driven by a source voltage of 230 V, 50 Hz. Neglecting diode resistances, calculate : i) Average d.c. voltage ii) Average direct current iii) Frequency of output waveform.

Ans. : Given, $R_L = 100\ \Omega$, $E_{s(RMS)} = 230$ V, $R_f = 0$, $f = 50$ Hz

$$E_{sm} = \sqrt{2} \times E_{s(RMS)} = \sqrt{2} \times 230 = 325 \text{ V}$$

i) Average d.c. voltage

$$E_{DC} = \frac{2E_{sm}}{\pi} = \frac{2 \times 325}{\pi} = 206.9 \text{ V} \quad \text{... As } R_f = 0$$

ii) Average direct current

$$I_{DC} = \frac{2I_m}{\pi} \text{ where } I_m = \frac{E_{sm}}{R_L + 2R_f + R_s}$$

$$I_m = \frac{3.25}{100 + 0 + 0} = 3.25 \text{ A}$$

$$I_{DC} = \frac{2 \times 3.25}{\pi} = 2.06 \text{ A}$$

iii) Frequency of output waveform

$$= 2f = 2 \times 50 = 100 \text{ Hz}$$

1.16 : Filter

Q.29 Explain the need of the filter.

Ans. : • The output of a rectifier circuit is not pure d.c.; but it contains fluctuations or ripples, which are undesired.

- To minimize the ripple content in the output, filter circuits are used.
- **The filter is an electronic circuit composed of capacitor, inductor or combination of both and connected between the rectifier and the load so as to convert pulsating d.c. to pure d.c.**
- The filter circuits are connected between the rectifier and load, as shown in the Fig. Q.29.1.

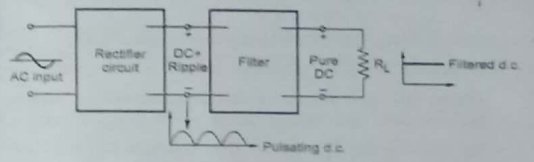


Fig. Q.29.1 Rectifier and filter

1.17 : Capacitor Filter Circuit

Important Points to Remember

- In capacitor filter circuit, a capacitor is connected in shunt with the load resistance. Looking from the rectifier side, the first element in the filter is capacitor hence it is also called capacitor input filter.

Q.30 Explain the operation of capacitor filter circuit with half wave rectifier.

Ans. : • The circuit diagram of half wave rectifier with shunt capacitor filter is shown in the Fig. Q.30.1.

- During the positive quarter cycle of the input, the capacitor C charges to peak value of the input i.e. E_{sm}. This is point A as shown in the Fig. Q.30.2.
- When input decreases, the C remains charged at E_{sm} and diode gets reverse biased.

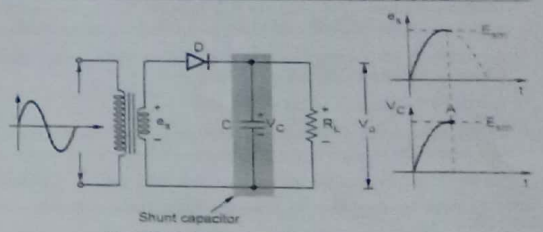


Fig. Q.30.1 Shunt capacitor filter with HWR

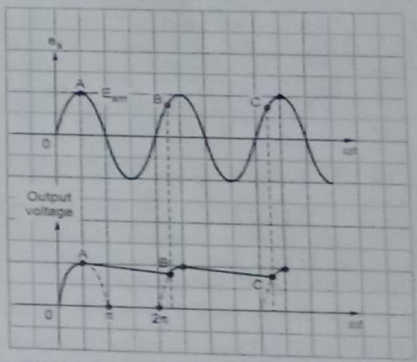


Fig. Q.30.2 Waveforms of shunt capacitor filter with HWR

- The capacitor C supplies the load R_L and starts discharging.
- Due to large time constant, capacitor discharges very little from E_{sm}.

- The capacitor supplies load for full negative half cycle and next part of positive half cycle till input is less than capacitor voltage.
- At point B, the capacitor starts charging as diode gets forward biased as input exceeds capacitor voltage.
- The point B is shown in the Fig. Q.30.3.
- As the discharging of capacitor is very small and charging time is very small, the ripples in the output get reduced considerably.
- The input and output waveforms are shown in the Fig. Q.30.3.

Q.31 Explain the operation of capacitor filter circuit with full wave rectifier.

Ans. :

- The Fig. Q.31.1 show the capacitor input filter with full wave rectifier.

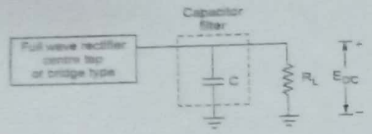


Fig. Q.31.1 Capacitor filter with full wave rectifier

- The full wave rectifier may be center tap or bridge rectifier.
- Immediately when power is turned on, the capacitor C gets charged through forward biased diode D_1 to E_{sm} during first quarter cycle of the rectified output voltage.
- In the next quarter cycle from $\frac{\pi}{2}$ to π, the capacitor starts discharging through R_L. Once capacitor gets charged to E_{sm}, the diode D_1 becomes reverse biased and stops conducting.
- So during the period from $\frac{\pi}{2}$ to π, the capacitor C supplies the load current. It discharges to point B shown in the Fig. Q.31.2.

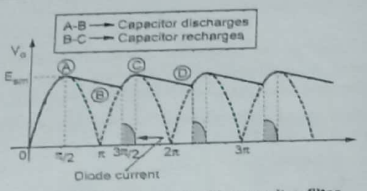


Fig. Q.31.2 FWR output with capacitor filter

- At point B, lying in the quarter π to $\frac{3\pi}{2}$ of the rectified output voltage, the input voltage exceeds capacitor voltage, making D_1 forward biased. This charges capacitor back to E_{sm} at point C.
- The time required by capacitor C to charge to E_{sm} is quite small and only for this period, diode D_2 is conducting.
- Again at point C, diode D_2 stops conducting and capacitor supplies load and starts discharging upto point D in the next quarter cycle of the rectified output voltage as shown in the Fig. Q.31.2. At this point, the diode D_1 conducts to charge capacitor back to E_{sm}. The diode currents are shown shaded in the Fig. Q.31.2.
- When the capacitor is discharging through the load resistance R_L both the diodes are non-conducting. The capacitor supplies the load current.

The operation remains same if full wave rectifier with two diodes is replaced with bridge rectifier. In a bridge rectifier, C charges through D_1 and D_2 in one half cycle and it recharges through D_3 and D_4 in next half cycle.

Q.32 Derive the expression for the ripple factor of rectifier using a capacitor filter.

Ans. :

- Let T = Time period of the a.c. input voltage

$\frac{T}{2}$ = Half of the time period

T_1 = Time for which diode is conducting

T_2 = Time for which diode is non-conducting

- During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant $R_L C$ is very large, discharging process is very slow and hence $T_2 >> T_1$.
- Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the Fig. Q.32.1.

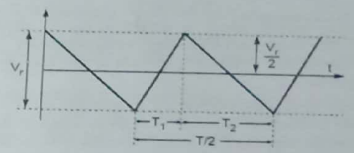


Fig. Q.32.1 Triangular approximation of ripple voltage

- For triangular assumption the r.m.s. value of the ripple voltage is given by,

$$V_{r(rms)} = \frac{V_r}{2\sqrt{3}} \quad \text{... As triangular} \quad \text{... (1)}$$

- During the time interval T_2, the capacitor C is discharging through the load resistance R_L. The charge lost is, $Q = CV_r$
- But $i = \frac{dQ}{dt}$ hence $Q = \int_0^{T_2} i\,dt = I_{DC}\,T_2$ as integration gives average or d.c. value

- Hence $I_{DC}\,T_2 = CV_r$ i.e $V_r = \frac{I_{DC}\,T_2}{C}$
- Now, $T_1 + T_2 = \frac{T}{2}$ and $T_2 >> T_1$ hence $T_1 + T_2 \approx T_2 = \frac{T}{2}$ where $T = \frac{1}{f}$

$$\therefore \quad V_r = \frac{I_{DC}}{C}\left[\frac{T}{2}\right] = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2\,fC}$$

- But $I_{DC} = \frac{E_{DC}}{R_L}$

$$\boxed{V_r = \frac{E_{DC}}{2\,f\,C\,R_L} = \text{Peak to peak ripple voltage}} \quad \text{... For full wave}$$

- The ripple factor is defined as the ratio of r.m.s. value of the a.c. component to the d.c. component. Hence the ripple factor of the capacitor filter with full wave rectifier is,

$$\text{Ripple factor} = \frac{V_{r(rms)}}{E_{DC}} = \frac{1}{4\sqrt{3}\,f\,C\,R_L} \quad \text{... For full wave}$$

- For **half wave rectifier** with capacitor input filter the ripple factor is,

$$\therefore \quad \text{Ripple factor} = \frac{1}{2\sqrt{3}\,f\,C\,R_L} \quad \text{... For half wave}$$

Important Points to Remember

- The ripple factor for capacitor input filter is,

Ripple factor (γ) = $\frac{1}{4\sqrt{3}\,f\,C\,R_L}$ for full wave

and $\gamma = \frac{1}{2\sqrt{3}\,f\,C\,R_L}$ for half wave

- The d.c. output voltage from a **capacitor filter is,**

$$E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{4fC}\right] \text{ for full wave}$$

and $$E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{2fC}\right] \text{ for half wave}$$

- The **ripple voltage** present in the output with capacitor filter is,

$$V_{r(RMS)} = \frac{I_{DC}}{4\sqrt{3}fC} \text{ volts for full wave}$$

and $$V_{r(RMS)} = \frac{I_{DC}}{2\sqrt{3}fC} \text{ volts for half wave}$$

- The r.m.s. ripple voltage is given by,

$$V_{r(RMS)} = E_{DC} \times \text{Ripple factor}$$

Q.33 State the advantages and disadvantages of capacitor filter.

Ans. : • The **advantages** of capacitor input filter are,

1. Less number of components.
2. Low ripple factor hence low ripple voltage.
3. Suitable for high voltage at small load currents.

• The **disadvantages** of capacitor input filter are,

1. Ripple factor depends on load resistance,
2. Not suitable for variable loads as ripple content increases as R_L decreases.
3. Regulation is poor.
4. Diodes are subjected to high surge currents hence must be selected accordingly.

1.18 : LC Filter or Choke Input Filter

Q.34 Explain the operation of choke input filter. State the expression for its ripple factor.

Ans. : A filter which uses one inductor and one capacitor is called LC filter. The filter element looking from the rectifier side is an inductor hence it is also called choke input filter or L-section filter.

• The Fig. Q.34.1 shows the choke input filter.

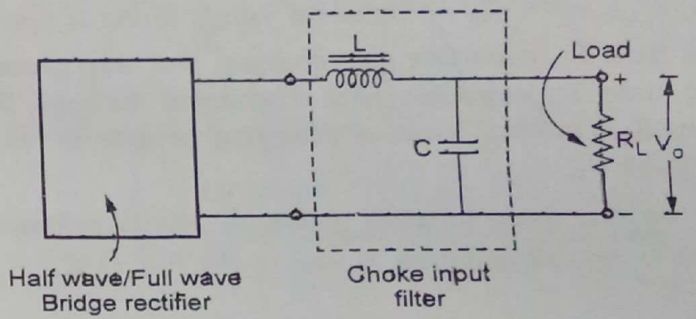


Fig. Q.34.1

- The rectifier output which is pulsating d.c. is applied to the choke L. The inductor offers very small resistance to d.c. and hence it allows d.c. component to pass to the load and it blocks a.c. component.
- Most of the ripples are blocked by an inductor but the remaining ripples are blocked by capacitor C. It offers small reactance to a.c ripples and as connected in shunt with the load, it bypasses the remaining ripples.
- The capacitor C offers high reactance to d.c. hence it blocks d.c component.
- Thus due to X_L and X_C reactances of L and C, almost pure d.c component is available to the load. Due to the double filtering effect, the output of this filter is very smooth.
- Its ripple factor is given by,

$$\gamma = \frac{1}{6\sqrt{2}\,\omega^2 LC}$$

... $\omega = 2\pi$

- It can be seen that the ripple factor is not dependent on the load resistance, which is its important advantage. It remains constant at all the loads.

• The Fig. Q.34.2 shows the waveforms of LC filter.

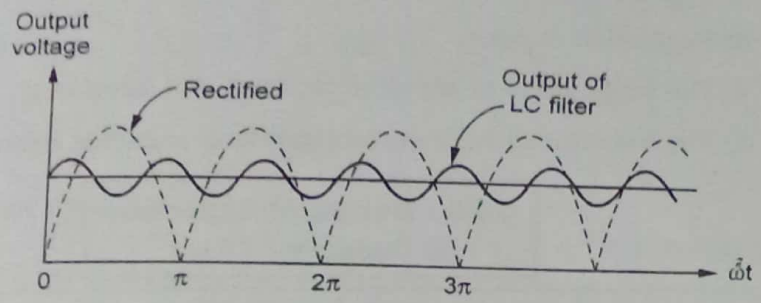


Fig. Q.34.2 Waveforms ac LC filter

This filter has good regulation and is suitable for all the loads, heavy as well as light loads.

Q.35 What is the necessity of bleeder resistance in LC filter ?

Ans. : Necessity of bleeder resistance : The basic requirement of an inductor is that the current through it must be continuous and not interrupted.

• If current through L is interrupted, it develops large back e.m.f. which may exceed PIV rating of the diodes and voltage rating of capacitor C. This may damage diodes and capacitor.

• To avoid this, inductor L must carry minimum current all the time continuously without any interruption. For this purpose a resistance R_B is connected across the output terminals, which is called **bleeder resistance.**

• The bleeder resistance is shown in the Fig. Q.35.1.

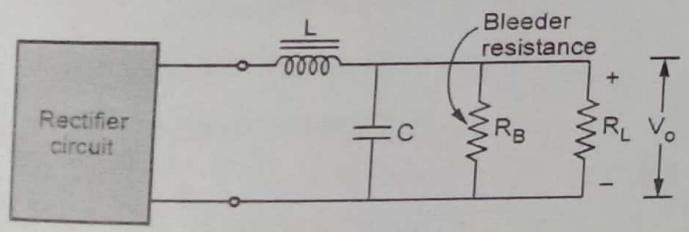


Fig. Q.35.1 LC filter with bleeder resistance

1.19 : π Filter or CLC Filter

Q.36 Explain the operation of π filter. State the expression for its ripple factor.

Ans. : • A filter which uses two capacitors and one inductor, is called CLC filter. The arrangement looks like a greek letter π (pi) hence is it is also called π filter.

• The capacitors are connected in shunt while an inductor is connected in series between the two shunt capacitors as shown in the Fig. Q.36.1.

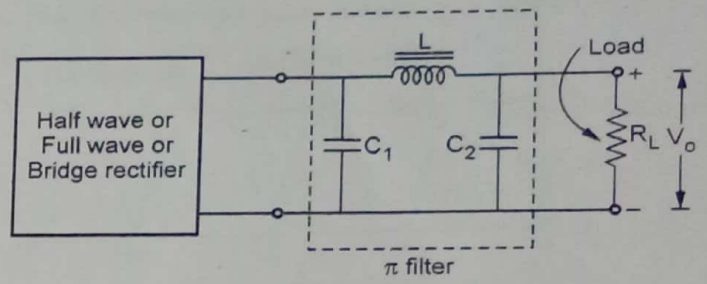


Fig. Q.36.1

• The rectifier output is given to the capacitor C_1 which is connected in parallel with the output of the rectifier. This capacitor offers very low reactance to the a.c. component but blocks d.c. component. Hence capacitor C_1 bypasses most of the a.c. component.

• The d.c. component then reaches to the choke L. The choke L offers very high reactance to a.c. component and very low reactance (almost zero) to d.c. So it blocks a.c. component and does not allow it to reach to load while it allows d.c. component to pass through it.

• The capacitor C_2 now allows to pass remaining a.c. component by offering very low reactance to a.c. ripples. Thus almost pure d.c. component reaches to the load.

- The ripple factor for this filter is,

$$\gamma = \frac{\sqrt{2}}{8\omega^3 LC_1 C_2 R_L} \quad \ldots \omega = 2\pi f$$

- It can be seen that the ripple factor increases as R_L decreases i.e. load current increases. Thus this filter is not suitable for high load currents hence it is preferred for light loads.
- The Fig. Q.36.2 shows the waveforms of π (Pi) filter.

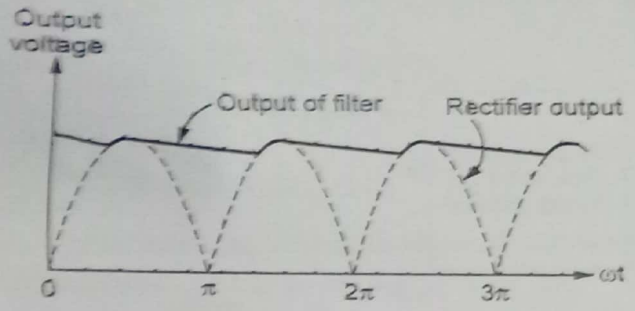


Fig. Q.36.2 Waveforms of π filter

- The output of this filter is very smooth but it is suitable only for light loads.

Q.37 State the advantages and limitations of π filter.

Ans. : • The various advantages of π filter are,

1) The ripple factor is much smaller than LC filter.
2) Higher d.c. output voltage at high load currents can be obtained.
3) The output is very smooth.
4) Easy from design point of view.
5) Useful for light loads.

- The disadvantages of π filter are,

1) It is bulky due to more number of filter components.

2) Higher PIV rating for the diodes is required.
3) Regulation is poor.
4) The large value of input capacitor C_1 in necessary.
5) The inductor of high current rating is required hence costly.

1.20 : Design of Capacitor in Capacitor Filter

Important Points To Remember

- Consider the path of the output voltage with ripple of rectifier with capacitor filter as shown in the Fig. 1.2.

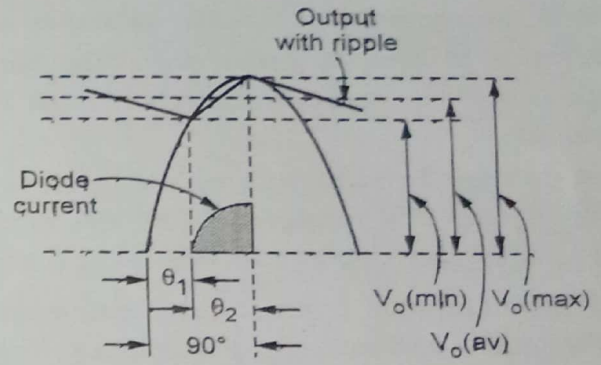


Fig. 1.2

V_T = Peak to peak ripple voltage

f = Input frequency

t_1 = Capacitor discharge time

t_2 = Capacitor charging time

From Fig. 1.2,

$$\theta_1 = \sin^{-1}\left[\frac{V_o\,(min)}{V_o\,(max)}\right]$$

$$\theta_2 = 90° - \theta_1$$

$$T = \frac{1}{f} \text{ and } t_1 + t_2 = T$$

$$t_2 = \frac{\theta_2 T}{360°}$$

For **half wave**, $t_1 = T - t_2$

For **full wave**, $t_1 = \frac{T}{2} - t_2$

$$\therefore \quad \boxed{C = \frac{I_L + 1}{V_r}}$$

For approximate calculations,

For **half wave**, $t_1 \approx T$

For **full wave**, $t_1 \approx \frac{T}{2}$

Q.38 The half wave rectifier d.c power supply is to supply 32 V to a 1 kΩ load. The peak to peak ripple voltage is not to exceed 10 % of average output voltage. If input frequency is 50 Hz, design the filter capacitor value.

Ans. :

$$V_o(av) = E_{DC} = 32 \text{ V}$$

$$\therefore \quad V_r = 10 \text{ \% of } V_o(av) = 3.2 \text{ V}$$

$$V_o(min) = V_o(av) - \frac{V_r}{2} = 30.4 \text{ V}$$

$$V_o(max) = V_o(av) + \frac{V_r}{2} = 33.6 \text{ V}$$

$$\theta_1 = \sin^{-1}\left[\frac{V_o(min)}{V_o(max)}\right] = 64.79°$$

$$\theta_2 = 90° - \theta_1 = 25.21°, \; T = \frac{1}{f} = 0.02 \text{ sec}$$

$$\therefore \quad t_2 = \frac{\theta_2 T}{360°} = \frac{25.21°}{360°} \times 0.02 = 1.4 \text{ msec}$$

$$\therefore \quad t_1 = T - t_2 = 0.02 - 1.4 \times 10^{-3} = 18.6 \text{ msec}$$

$$I_L = \frac{V_o(av)}{R_L} = \frac{32}{1 \times 10^3} = 32 \text{ mA}$$

$$\therefore \quad C = \frac{I_L t_1}{V_r} = \frac{32 \times 10^{-3} \times 18.6 \times 10^{-3}}{3.2} = 186 \; \mu\text{F}$$

Q.39 If in the Q.38, half wave rectifier is replaced by full wave rectifier, find the new capacitor value.

Ans. : All calculation till t_2 remain same.

$$t_1 = \frac{T}{2} - t_2 = \frac{0.02}{2} - 1.4 \times 10^{-3} = 8.6 \text{ msec}$$

$$I_L = \frac{32}{1 \times 10^3} = 32 \text{ mA}$$

$$\therefore \quad C = \frac{I_L t_1}{V_r} = 86 \; \mu\text{F}$$

1.21 : Clipping Circuits

Q.40 Define clipper circuit. State its types.

Ans. : • The circuits which are used to clip off (remove) unwanted portion of the waveform, without distorting the remaining part of the waveform are called **clipper circuits** or **clippers.**

- The two types of clipper circuits are, i) Sries cippers and ii) Shunt clippers
- In series clipper the diode is connected in series with the load while in shunt clipper the diode is connected in parallel with the load.

Q.41 Draw the circuit of series positive clipper and explain its operation alongwith the waveforms.

Ans. : • The Fig. Q.41.1 shows positive series clipper circuit in which diode direction is opposite to that in negative series clipper circuit.

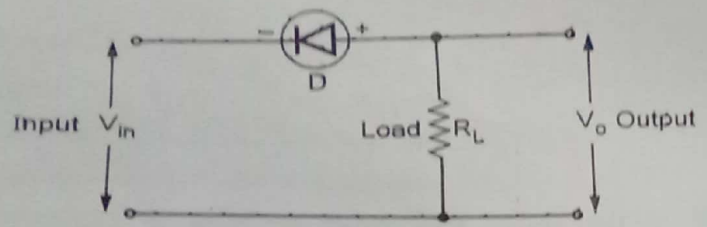
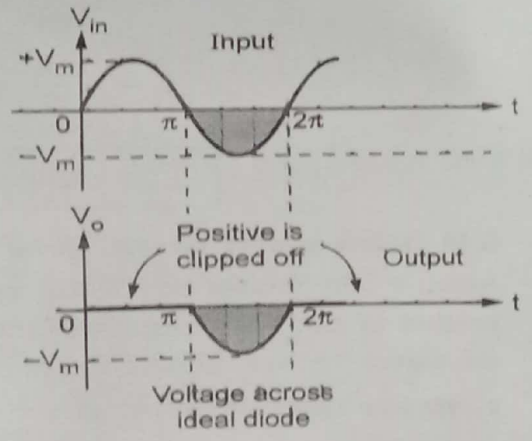


Fig. Q.41.1 Positive series clipper

- For positive half cycle of input, $V_{in} > 0$ V and diode is reverse biased. Hence it acts as open circuit and $V_o \approx 0$ V.
- For negative half cycle, when $V_{in} < 0$, the diode conducts.
- Assuming ideal diode, the output voltage V_o available is same as the input voltage.
- Thus entire negative half cycle of input is available at the output.
- Thus positive series clipper clips off the positive part of the input waveform.
- The output waveforms for sinusoidal input are shown in the Fig. Q.41.2.



Sinusoidal input

Fig. Q.41.2 Waveforms of series positive clipper

Q.42 Draw the circuit of series negative clipper and explain its operation alongwith the waveforms. Draw its transfer characteristics.

Ans. : • The circuit which clipps off the negative portion of input is called negative clipper.

- Consider a series negative clipper shown in the Fig. Q.42 where diode is connected in series with the load.

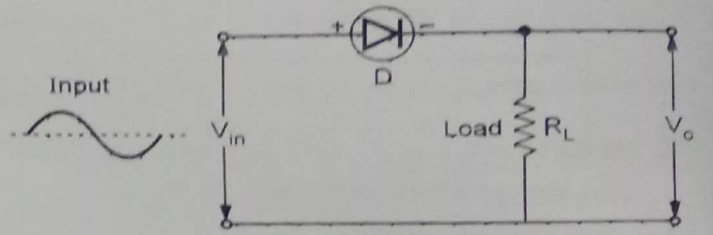
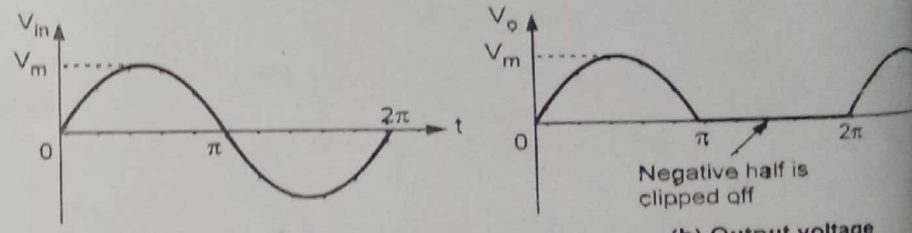


Fig. Q.42.1 Negative series clipper

- For a positive half cycle, the diode D is forward biased. He the entire positive half cycle is available across the load resist R_L.
- While for a negative half cycle, diode D is reverse biased hence will not conduct at all. Hence there will not be any volt available across resistance R_L. Hence the negative half cycl input voltage gets clipped off.
- The input waveform and the corresponding output volt waveform is shown in the Fig. Q.42.2.



(a) Input voltage **(b) Output voltage**

Fig. Q.42.2 Waveforms of series negative clipper

- The graph of output variable against input variable of the ci is called transfer characteristics of the circuit.
- For the negative series clipper, the graph of V_o against V_{in} transfer characteristics.

- The mathematical equation for such a graph for negaive series clipper, **assuming ideal diode** is given by,

$V_o = V_{in}$	... For $V_{in} \geq 0$
$V_o = 0,$	... For $V_{in} < 0$

- The graph showing the transfer characteristics is shown in the Fig. Q.42.3.

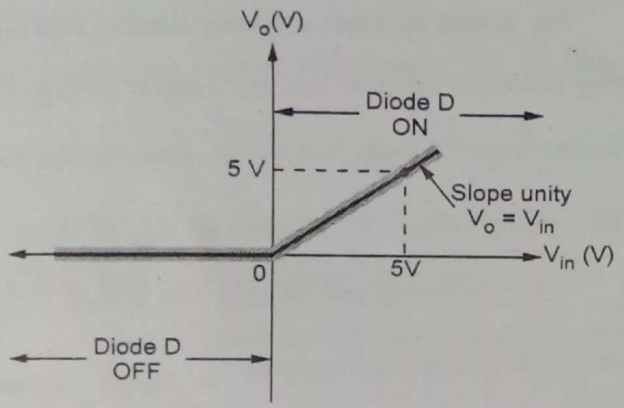


Fig. Q.42.3 Transfer characteristics

Q.43 Draw the parallel positive clipper and explain its operation alongwith the waveforms.

Ans. : • In a parallel clipper circuit, the diode is connected across the load terminals.

- The Fig. Q.43.1 shows the basic parallel positive clipper circuit in which diode D is connected across the load resistance R_L. The resistance R_1 is current controlling resistance.
- During **positive half cycle** of the input V_{in}, the diode D becomes **forward biased** and remains forward biased for the entire positive half cycle of the input.
- As ideal diode acts as short circuit when forward biased hence the current I flows entirely through diode D. The drop across short circuit diode is zero. Hence output voltage $V_o = 0$ V for entire positive half cycle.

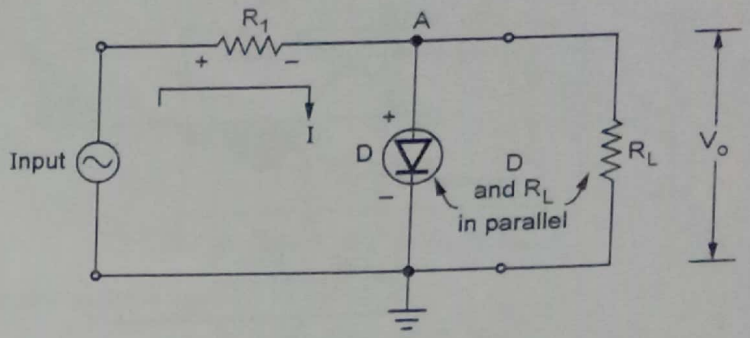


Fig. Q.43.1 Parallel positive clipper

- Thus positive half cycle gets clipped off.
- During **negative half cycle** of input, the diode is **reverse biased** and acts as open circuit. The entire current flows through R_L as shown in the Fig. Q.43.2.

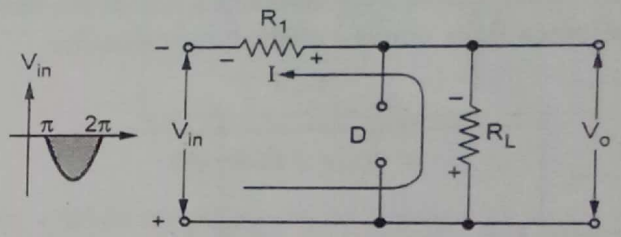


Fig. Q.43.2 Operation during negative half cycle

- Hence $V_o = \frac{V_{in} R_L}{R_L + R_1}$ using potential divider rule.
- Thus the output voltage V_o is same as V_{in}, for $R_1 << R_L$.
- Thus the entire negative half cycle of V_{in} gets reproduced at the output.
- The waveforms are shown in the Fig. Q.43.3.

- The mathematical equation for such a graph for negaive series clipper, **assuming ideal diode** is given by,

$V_o = V_{in}$	... For $V_{in} \geq 0$
$V_o = 0,$	... For $V_{in} < 0$

- The graph showing the transfer characteristics is shown in the Fig. Q.42.3.

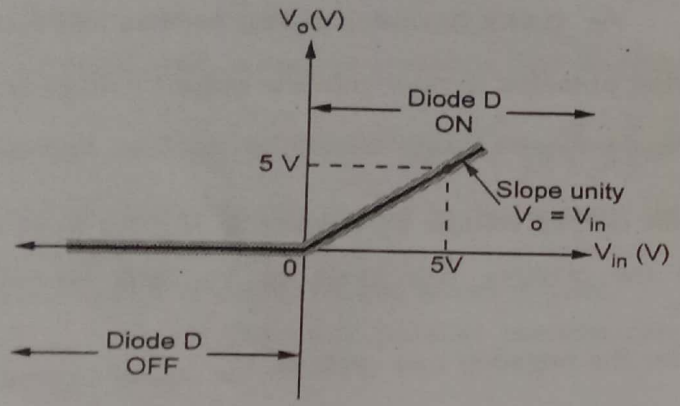


Fig. Q.42.3 Transfer characteristics

Q.43 Draw the parallel positive clipper and explain its operation alongwith the waveforms.

Ans. : • In a parallel clipper circuit, the diode is connected across the load terminals.

- The Fig. Q.43.1 shows the basic parallel positive clipper circuit in which diode D is connected across the load resistance R_L. The resistance R_1 is current controlling resistance.
- During **positive half cycle** of the input V_{in}, the diode D becomes **forward biased** and remains forward biased for the entire positive half cycle of the input.
- As ideal diode acts as short circuit when forward biased hence the current I flows entirely through diode D. The drop across short circuit diode is zero. Hence output voltage $V_o = 0\,V$ for entire positive half cycle.

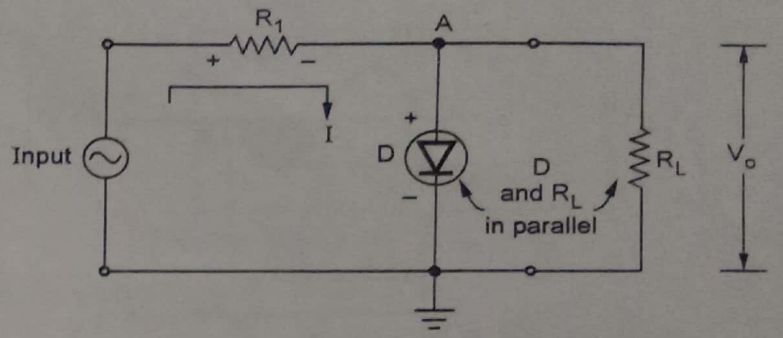


Fig. Q.43.1 Parallel positive clipper

- Thus positive half cycle gets clipped off.
- During **negative half cycle** of input, the diode is **reverse biased** and acts as open circuit. The entire current flows through R_L as shown in the Fig. Q.43.2.

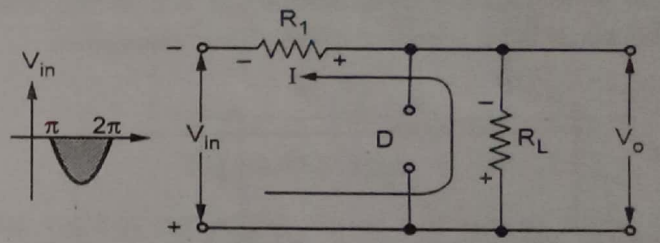


Fig. Q.43.2 Operation during negative half cycle

- Hence $V_o = \dfrac{V_{in} R_L}{R_L + R_1}$ using potential divider rule.
- Thus the output voltage V_o is same as V_{in}, for $R_1 << R_L$.
- Thus the entire negative half cycle of V_{in} gets reproduced at the output.
- The waveforms are shown in the Fig. Q.43.3.

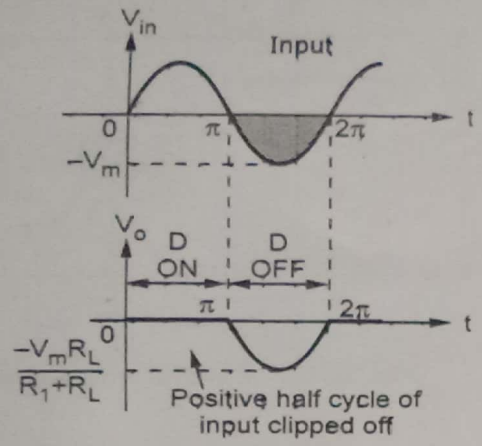


Fig. Q.43.3 Waveforms for parallel positive clipper

Q.44 Draw the parallel negative clipper and explain its operation alongwith the waveforms.

Ans. : • The Fig. Q.44.1 shows the basic parallel negative clipper circuit in which diode D is connected across the load resistance R_L. The resistance R_1 is current controlling resistance.

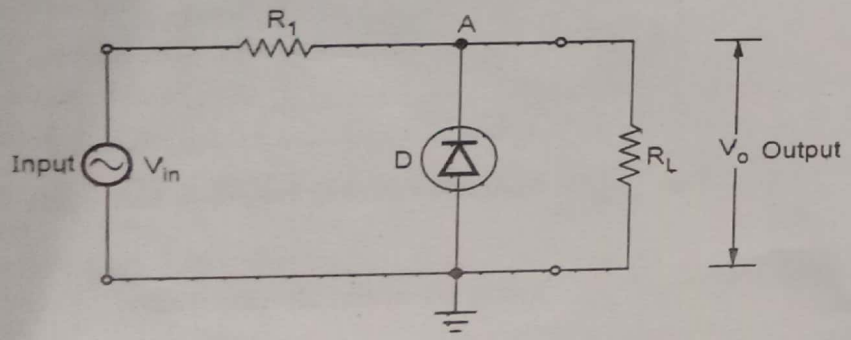


Fig. Q.44.1 Parallel negative clipper

• When V_{in} is positive then the diode is reversed biased and acts as an open circuit. The circuit is shown in the Fig. Q.44.2.

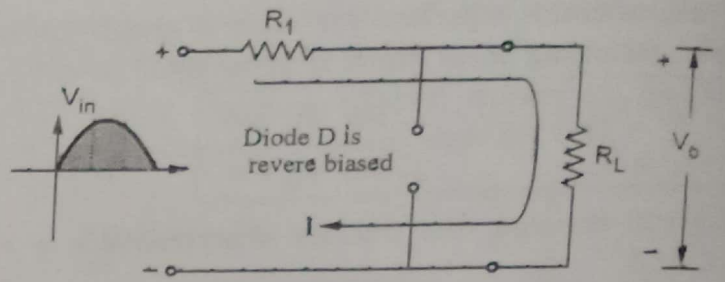


Fig. Q.44.2 Operation during positive half cycle

• Applying potential divider rule the output voltage is given by,

• $V_o = V_{in}\left[\frac{R_L}{R_1 + R_L}\right] \approx V_{in}$ ... $R_1 << R_L$

• Thus the output voltage V_o is same as V_{in}, for $R_1 << R_L$.

• Hence the positive half cycle of V_{in} gets reproduced at the output.

• Consider the negative half cycle of V_{in}.

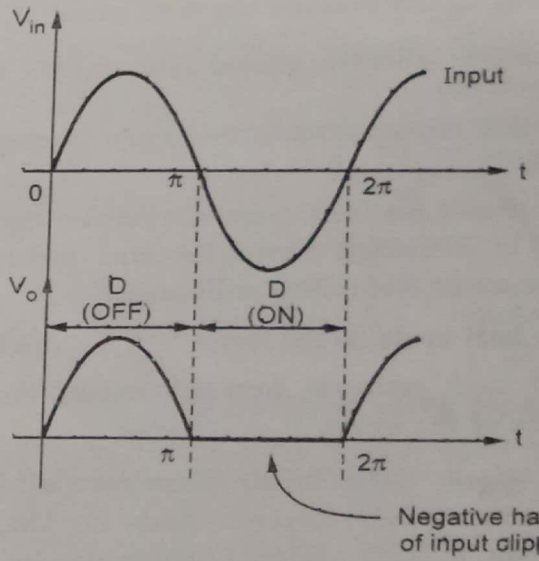


Fig. Q.44.3 Waveforms for parallel negative clipper

- As the diode is forward biased in this half cycle, the entire current passes through the diode as it acts as a closed switch.
- The forward biased diode produces short circuit across the load.
- The voltage across short circuit is zero hence the output voltage is zero for the entire negative half cycle of the input.
- Thus the negative half cycle gets clipped off and circuit acts as a negative clipper.
- The overall input and output waveforms are as shown in the Fig. Q.44.3.

Q.45 Explain the working of biased shunt clipper along with its waveforms.

Ans. : • When a battery is introduced in series with the diode to achieve the clipping above or below the certain reference voltage in a shunt clipper then it is called **biased shunt clipper.**

- The Fig. Q.45.1 shows the basic parallel positive clipper circuit with reference voltage.

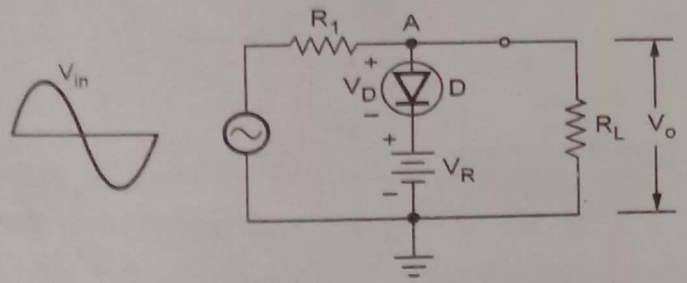


Fig. Q.45.1 Positive clipper with reference voltage

- The operation for **positive half cycle** of the input can be divided into two cases.

Case 1 : When V_{in} is positive but less than V_R, the diode D is reverse biased and acts as open circuit. The equivalent circuit is as shown in the Fig. Q.45.2.

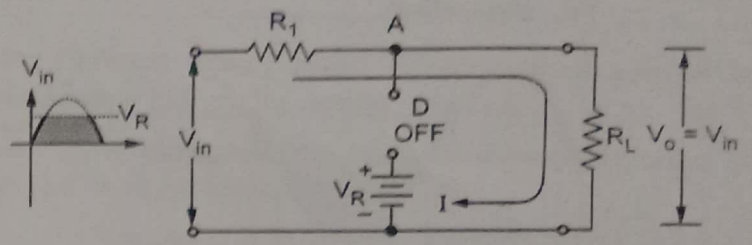


Fig. Q.45.2 $0V < V_{in} < V_R$

- Hence the output voltage is given by,

$$V_o = V_{in} \frac{R_L}{R_1 + R_L} = V_{in} \quad \text{... for } R_1 \ll R_L$$

Case 2 : when V_{in} becomes greater than V_R, the diode D becomes **forward biased** and acts as short circuit. This is shown in the Fig. Q.45.3.

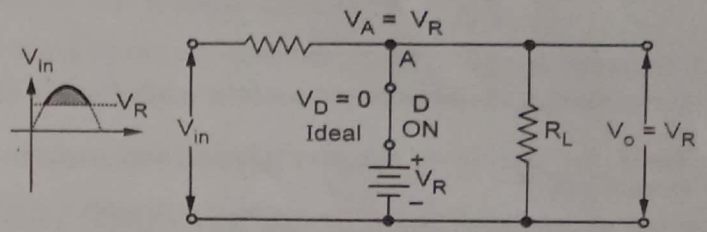


Fig. Q.45.3 $V_{in} > V_R$

- The output voltage now is same as voltage of node A which is V_R, as the drop across ideal ON diode is zero.

$$\therefore \quad V_o = V_R \quad \text{... for } V_{in} > V_R$$

- When V_o again becomes less than V_R, the diode D becomes OFF and $V_o \approx V_{in}$.
- For the entire **negative half cycle** of the input, $V_{in} < V_R$ hence diode D remains reverse biased. It acts as open circuit.
- Thus $V_o = V_{in}$ and the entire negative half cycle is reproduced at the output.
- The input and output waveforms are shown in the Fig. Q.45.4.

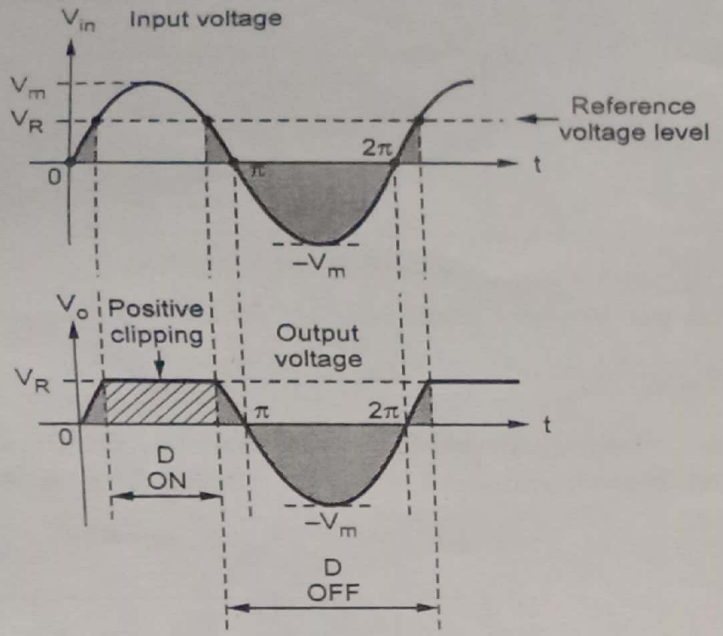


Fig. Q.45.4 Waveforms for positive biased shunt clipper

Q.46 Draw the circuit of two way clipper and explain its working with waveforms.

Ans. : • The circuit diagram of two way parallel clipper is shown in the Fig. Q.46.1.

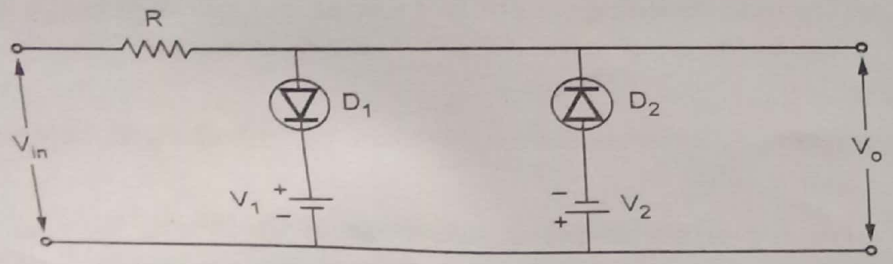


Fig. Q.46.1 Combinational clipper

• Assume that the input is purely sinusoidal in nature and diodes D_1 and D_2 are ideal diodes.

Positive half cycle of the input :

- When V_{in} goes positive till it becomes more than V_1, D_1 and both the diodes are reverse biased. And $V_o = V_{in}$.
- When $V_{in} > V_1$, then D_1 becomes forward biased and condu While D_2 remains reverse biased for the entire positive half cy of the input. Hence $V_o = V_1$.
- Thus when $V_{in} < V_1$, D_1 and D_2 are OFF and $V_o = V_{in}$.
- While when $V_{in} > V_1$, D_1 is ON and D_2 is OFF and $V_o = V_1$.

Negative half cycle of the input :

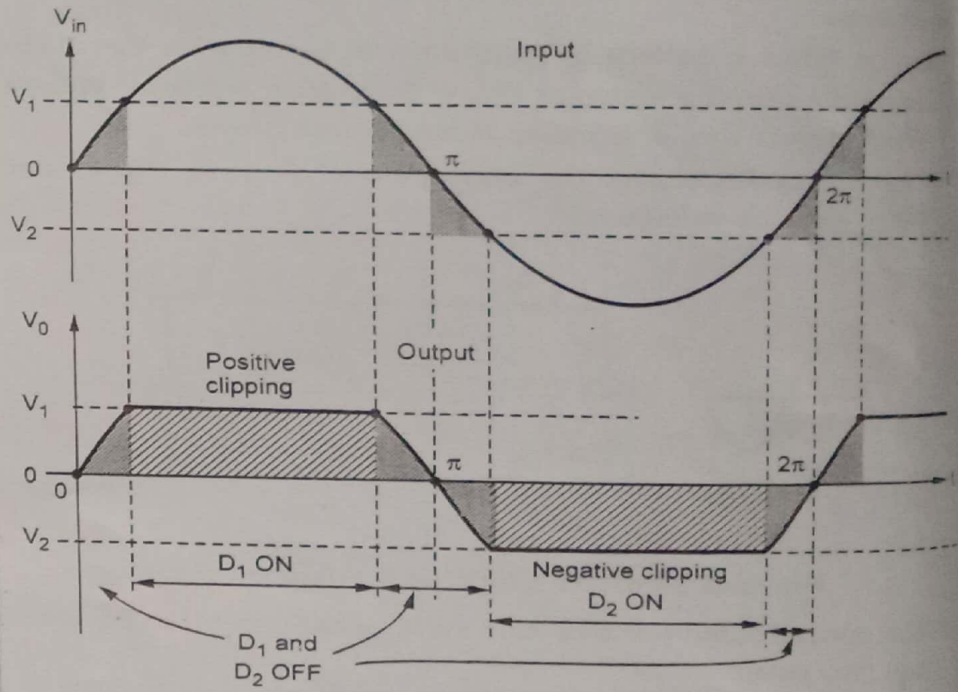


Fig. Q.46.2 Waveforms of two way clipper

- In the negative half cycle, as long as V_{in} is greater than V_2, th diode D_2 remains reverse biased. The D_1 remains OFF for th entire negative half cycle of the sinput.

- When V_{in} becomes less than V_2, the diode D_2 becomes forward biased and conducts. The diode D_1 is still OFF. Hence $V_o = V_2$. The output V_o is negative as the polarities of V_2 are opposite to that of V_1.
- Thus when $V_{in} > V_2$, D_1 and D_2 are OFF and $V_o = V_{in}$
- While when $V_{in} < V_2$, D_1 is OFF and D_2 is ON and $V_o = V_2$
- The input and output waveforms for the two way clipper are shown in the Fig. Q.46.2.

Q.47 Draw and explain the operation of zener diode shunt clipper.

Ans. : • The zener diode shunt clipper uses two back to back series connected zener diodes in shunt with the load resistance. This is shown in the Fig. Q.47.1

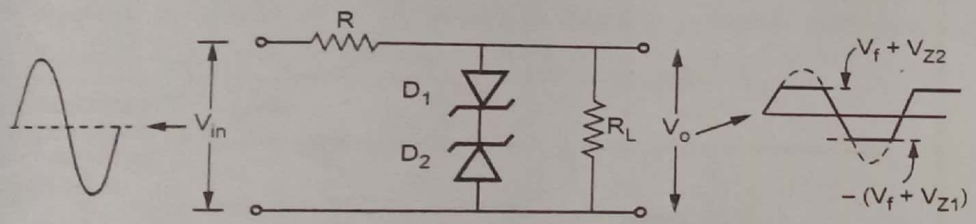


Fig. Q.47.1

- The voltage across forward biased zener diode is V_f while the voltage across reverse biased zener diode is V_Z.
- The zener voltage of D_1 is V_{Z1} white the zener voltage of D_2 is V_{Z2}.
- For positive half cycle, for sufficient input voltage, D_1 is forward biased while D_2 is in reverse breakdown. This limits the output voltage to $(V_f + V_{Z2})$.
- For negative half cycle, for sufficient negative voltage, D_2 is forward biased and D_1 is in reverse breakdown. This limits the output voltage to $-(V_f + V_{Z1})$.

- Using different zener voltage, different clipping levels in positive and negative half cycles can be obtained.
- This clipper eliminates the need of separate batteries which are required in shunt biased clippers.

1.22 : Clamping Circuits

Q.48 What is clamper ? Which are the two basic elements of clamper ? How clampers are classified ?

Ans. : • The circuits which are used to add a d.c. level as per the requirements to the a.c. output signal are called **clamper circuits**.

- The capacitor, diode and resistance are the three basic elements of a clamper circuit. The clamper circuits are also called **d.c. restorer** or **d.c. inserter circuits**.
- Depending upon whether the positive d.c. or negative d.c. shift is introduced in the output waveform, the clampers are classified as,

a) Negative clampers and b) Positive clampers.

Q.49 Draw a negative clamper circuit and explain its operation.

Ans. : • A negative clamper is shown in the Fig. Q.49.1.

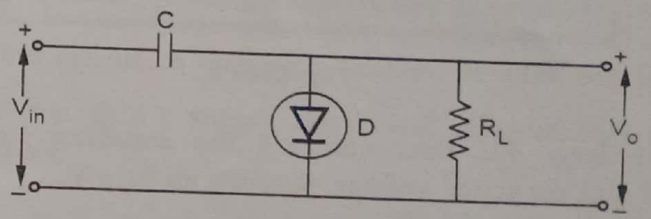


Fig. Q.49.1 Negative clamper

- During the first quarter of **positive cycle** of the input voltage V_{in}, the capacitor gets charged through **forward biased diode** D upto the maximum value V_m of the input signal V_{in}.
- The capacitor charging is almost instantaneous.

- The capacitor once charged to V_m, acts as a battery of voltage V_m because of its large time constant, as shown in the Fig. Q.49.2.

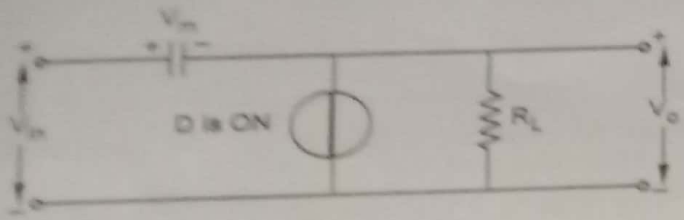


Fig. Q.49.2

- Thus when D is ON, the output voltage V_o is zero.
- As input voltage decreases after attaining its maximum value V_m, the capacitor remains charged to V_m and the diode D becomes reverse biased as shown in the Fig. Q.49.3.

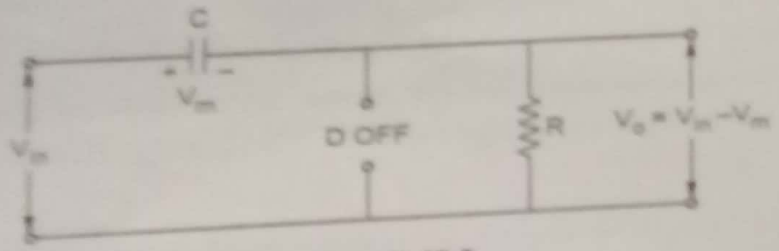


Fig. Q.49.3

- Due to large RC time constant the capacitor holds its entire charge and capacitor voltage remains as $V_C = V_m$.
- The output voltage V_o is now given by, $V_o = V_{in} - V_C = V_{in} - V_m$.
- This is as good as adding a negative d.c. level equal to $-V_m$ to the output.
- Assuming ideal diode, the input and output waveforms are shown in the Fig. Q.49.4.

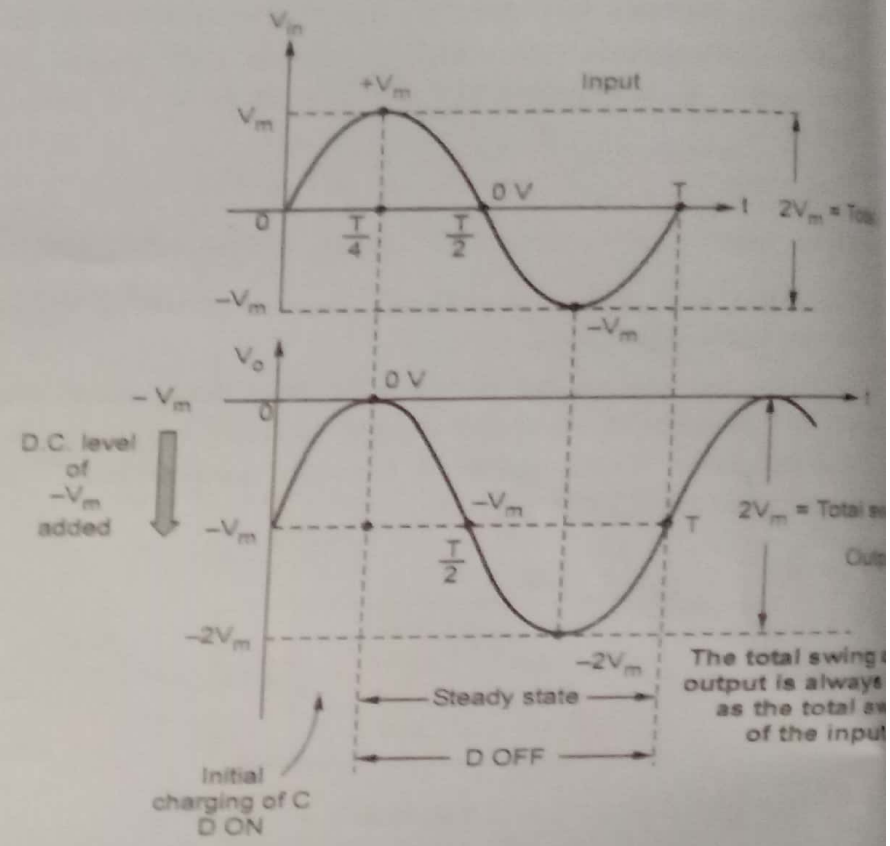


Fig. Q.49.4 Negative clamper waveforms

Q.50 Draw a positive clamper and explain its working alon the waveforms.

Ans. : • The positive clamper circuit is shown in the Fig. Q.5

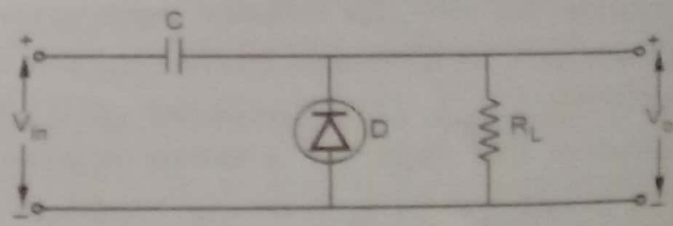


Fig. Q.50.1 Positive clamper

- During the first quarter of **negative half cycle** of the input voltage V_{in}, diode D gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value V_m of the input signal V_{in}, with the polarities as shown in the Fig. Q.50.2.

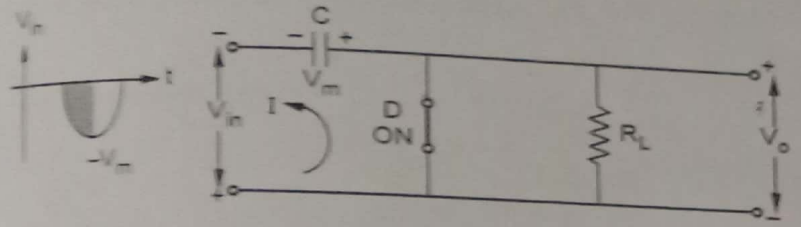


Fig. Q.50.2

- In the **positive half cycle**, the diode D is reverse biased. The capacitor starts discharging through R_L. But due to large time constant, it hardly gets discharged during positive half cycle of V_{in}. This is shown in the Fig. Q.50.3.

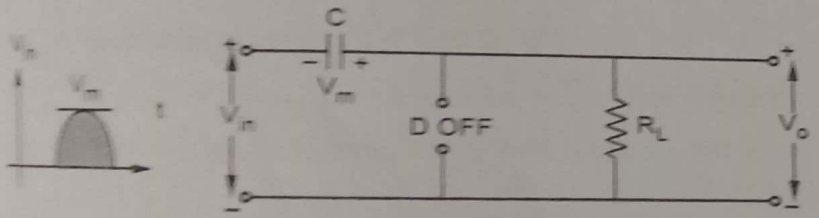


Fig. Q.50.3

- The capacitor holds its entire charge, all the time.
- Hence applying KVL, $V_o = V_{in} + V_m$.
- Assuming ideal diode, the input and output waveforms are drawn in the Fig. Q.50.4.

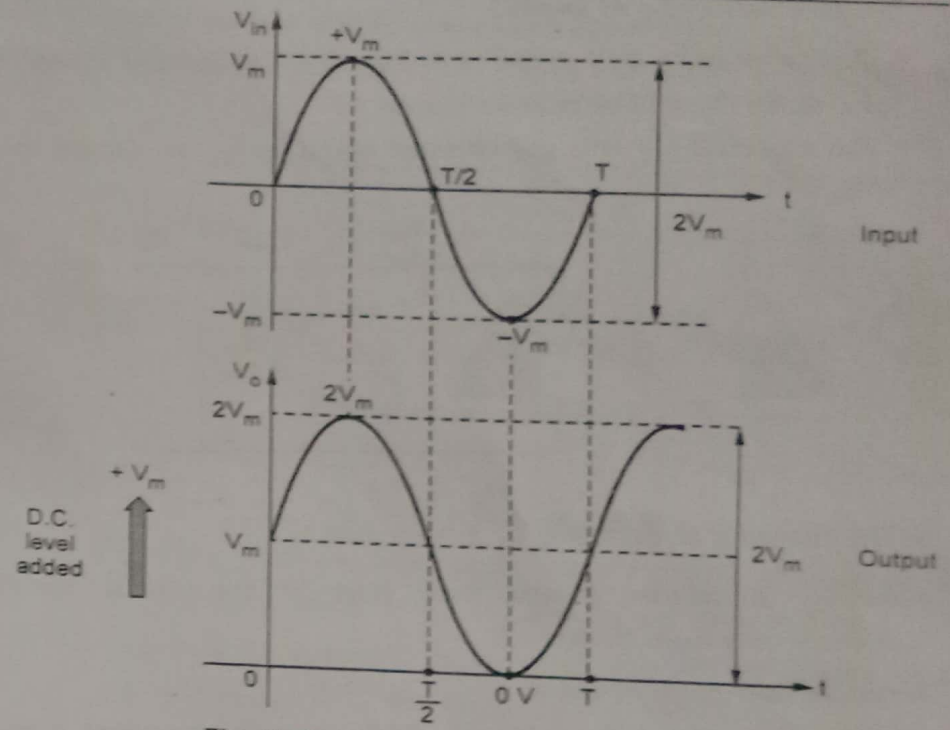


Fig. Q.50.4 Positive clamper waveforms

1.23 : Voltage Multiplier Circuits

Q.51 Draw the circuit of half wave voltage doubler and explain its working.

Ans. : • The Fig. Q.51.1 shows the circuit diagram of a **half wave** voltage doubler.

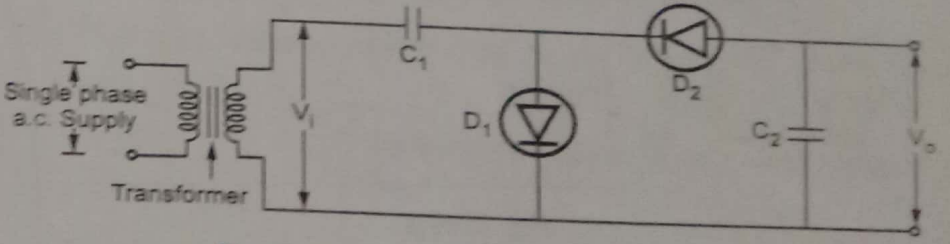


Fig. Q.51.1 Half wave voltage doubler

Positive half cycle of input :

- During positive half cycle of V_i, D_1 will be forward biased and the diode D_2 will be reverse biased.
- The capacitor C_1 will get charged equal to V_m as shown in the Fig. Q.51.2.

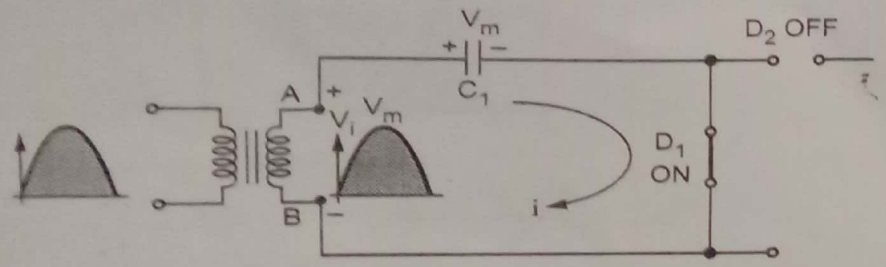


Fig. Q.51.2

- The charging of capacitor C_1 is very fast.
- As D_2 is reverse biased, next part of the circuit remains disconnected from the circuit.

Negative half cycle of input :

- During negative half cycle, the diode D_1 will be reverse biased and the diode D_2 will be forward biased.
- The capacitor C_1 remains charged at V_m. So the voltage V_m on C_1 adds to the input voltage.
- So capacitor C_2 will get charged equal to 2 V_m with the polarities as shown in Fig. Q.51.3.

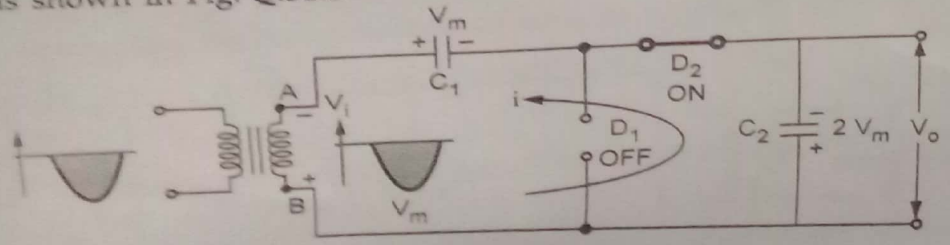


Fig. Q.51.3

- It retains this voltage as long as load is connected to the c
- Thus the ouput is double of the input hence the circuit is **voltage doubler.**

Q.52 Draw the circuit of full wave voltage doubler and expla working.

Ans. : • The Fig. Q.52.1 shows a full wave voltage doubler.

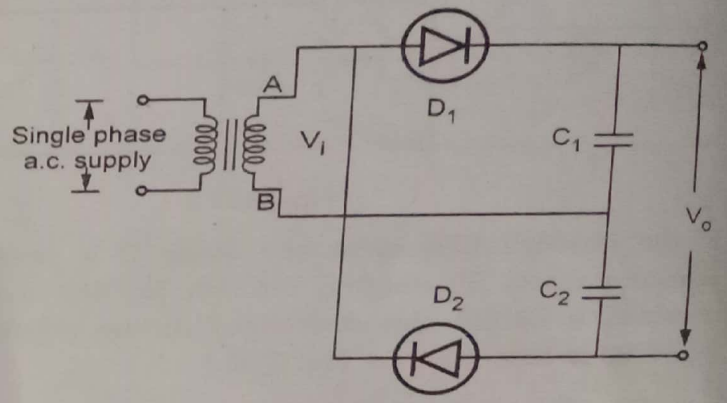


Fig. Q.52.1 Full wave voltage doubler

Positive half cycle of input :

- In the positive half cycle of the secondary voltage of transfo the diode D_1 is forward biased.
- Thus the capacitor C_1 charges through the forward biased d D_1, equal to V_m which is the peak of secondary transfo voltage, assuming ideal diodes.
- This is shown in the Fig. Q.52.2.

Negative half cycle of input :

- In the negative half cycle of the secondary voltage of transfor the diode D_2 is forward biased while the diode D_1 is rev biased.

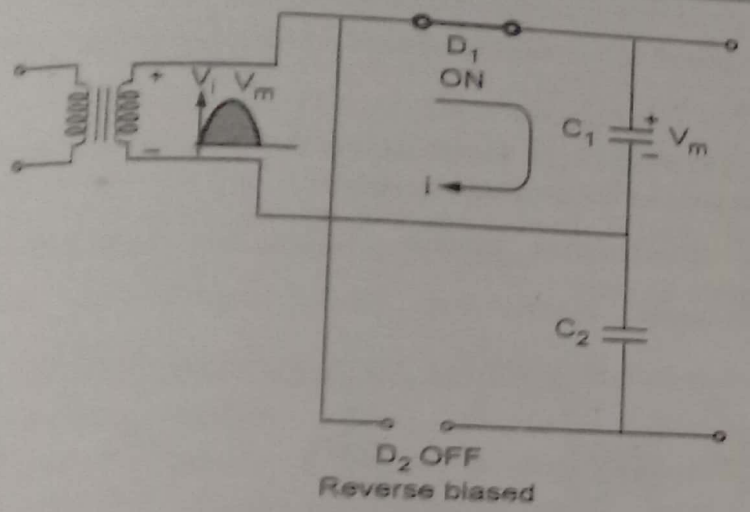


Fig. Q.52.2 Positive half cycle of input

- The capacitor C_2 gets charged equal to V_m with the polarity as shown in the Fig. Q.52.3.

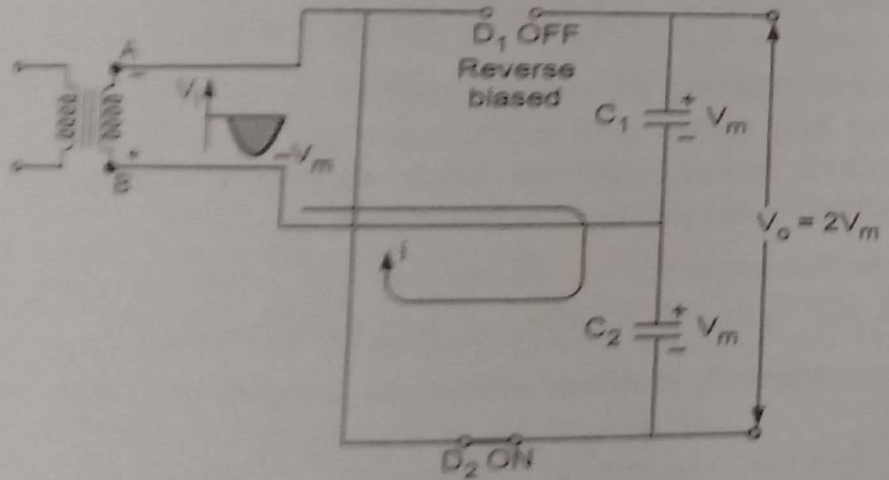


Fig. Q.52.3 Negative half cycle of input

- The output is taken across 2 capacitors in series.

$$V_o = V_{C1} + V_{C2} = V_m + V_m = 2V_m$$

- Thus the output is double of the input hence the circuit is called voltage doubler.

Q.53 Explain voltage tripler and voltage quadrupler.

Ans. : Voltage tripler circuit : The Fig. Q.53.1 shows a voltage tripler circuit.

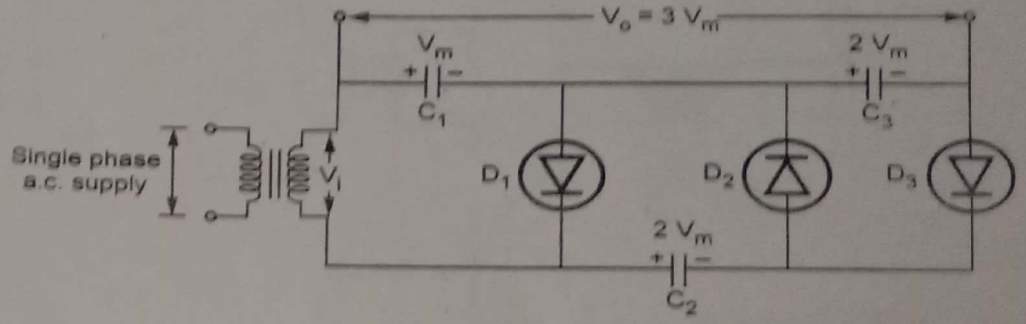


Fig. Q.53.1 Voltage tripler

- During **first positive half cycle** of the input, the diode D_1 becomes forward biased while D_2 and D_3 are reverse biased.
- The capacitor C_1 charges to V_m through the forward biased diode D_1 with the polarities as shown in the Fig. Q.53.2.

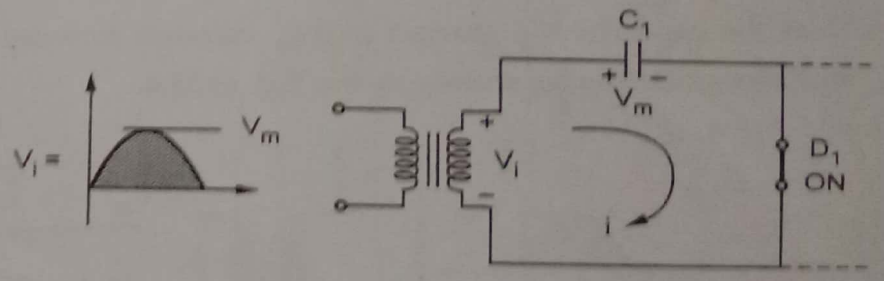


Fig. Q.53.2 C_1 charges to V_m through diode D_1

- During **next negative half cycle** of the input, the diode D_2 is forward biased.
- The capacitor C_1 holds its entire charge and its voltge remains at V_m.

- Hence the capacitor C_2 charges to $2V_m$ with the polarities as shown in the Fig. Q.53.3.

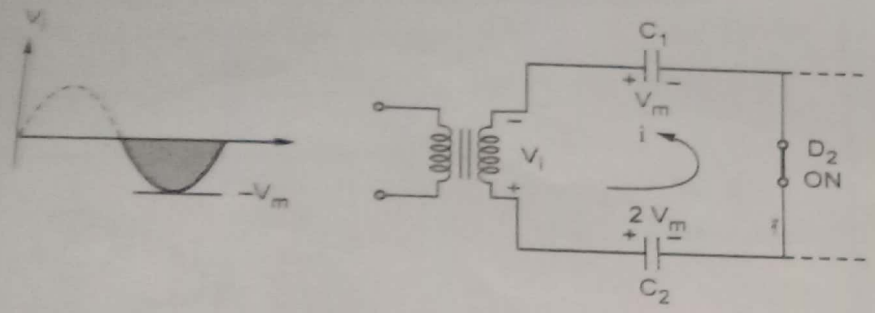


Fig. Q.53.3

- The diodes D_1 and D_3 are reverse biased.
- Applying KVL, $+V_m - V_{C2} + V_{C1} = 0$ i.e. $V_{C2} = V_m + V_{C1} = 2V_m$
- In the **next positive half cycle** of the input, the diode D_3 is forward biased because C_2 retains its charge and voltage across it to $2V_m$ while C_1 retains voltage across it to V_m.
- The diodes D_1 and D_2 are reverse biased.
- Thus the capacitor C_3 charges to $2V_m$ through forward biased D_3 with the polarities as shown in the Fig. Q.53.4.

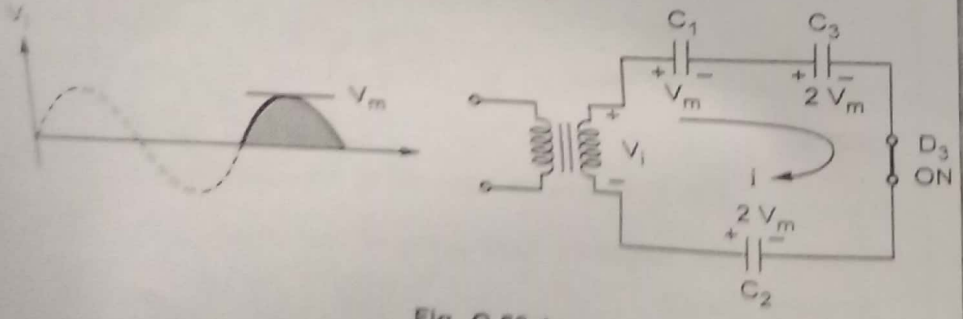


Fig. Q.53.4

- Applying KVL, $+V_m - V_m - V_{C3} + V_{C2} = 0$ i.e. $V_{C3} = V_{C2} = 2V_m$

- The output V_o is taken across the capacitors C_1 and C_3 i.e. $V_o = V_{C1} + V_{C3} = 3V_m$.
- Thus the output is three times the peak of the input voltage and circuit works as **voltage tripler.**

Voltage quadrupler circuit : The Fig. Q.53.5 shows a voltage quadrupler circuit.

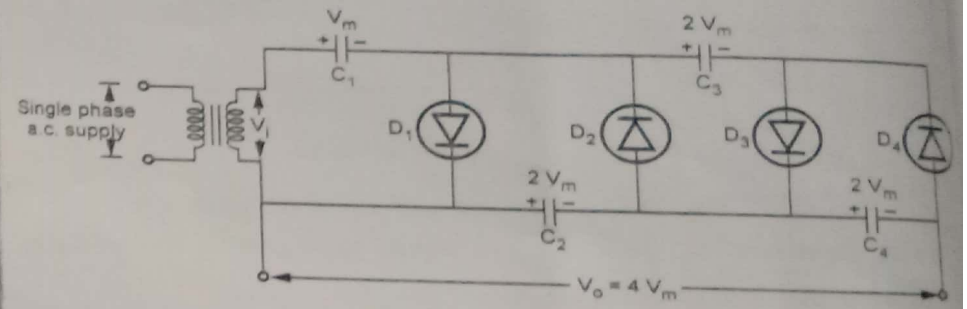


Fig. Q.53.5 Voltage quadrupler

- Analyse the circuit exactly similar to the voltage tripler for fi three half cycles and in the next half cycle the diode D_4 will forward biased with all other capacitors holding their char and hence the same voltages across them.
- Thus the capacitor C_4 charges to $2V_m$, with the polarity shown the Fig. Q.53.5 in a negative half cycle, through D_4.
- The output V_o is taken across the capacitors C_2 and C_4.

$$\therefore \quad V_o = V_{C2} + V_{C4} = 2V_m + 2V_m = 4V_m$$

Thus the output is four times the peak of the input voltage circuit works as **voltage quadrupler.**

1.24 : Reading Datasheet of Semiconductor Diode

Important Points To Remember

- The manufacturer of diode provides the detail information about the diode, in the form of datasheet. The various diode parameters are specified in the datasheet which help us to select the diode for an application circuit.

Q.54 Explain the various diode parameters specified in its datasheet.

Ans. : The various diode parameters specified in the datasheet are,

i) **Reverse saturation current** : The constant reverse current flowing through the diode, when it is reverse biased is called **reverse saturation current** of diode denoted as I_0.

- It is constant at constant temperature, though reverse voltage is increased till breakdown of diode occurs.

ii) **Reverse breakdown voltage** : When the reverse voltage is increased, at a certain value the breakdown of diode occurs and reverse current increases very sharply. This voltage is called reverse breakdown voltage and denoted as V_{BR}. The diode gets damaged due to breakdown.

iii) **Knee voltage** : A small forward voltage applied to a forward biased diode at which current starts increasing exponentially i.e. rapidly is called knee voltage of a diode.

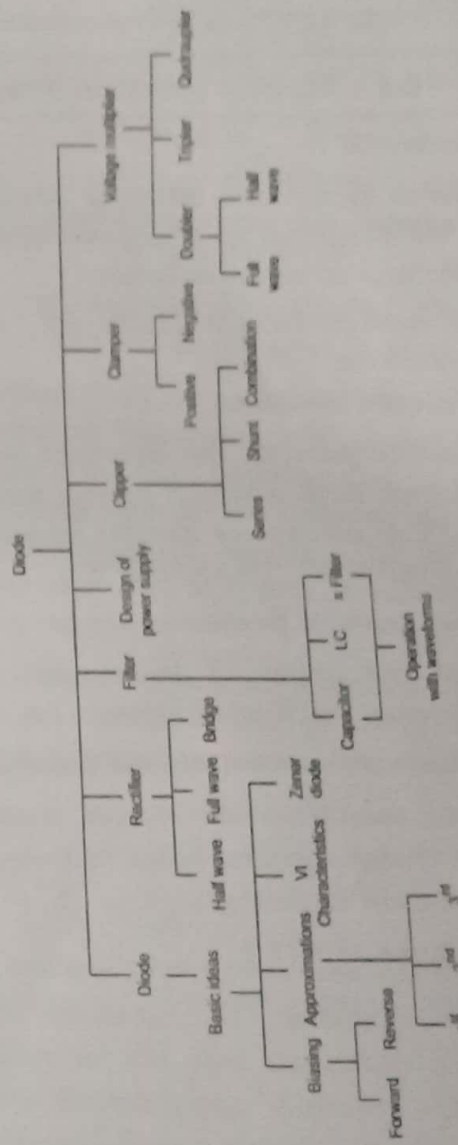
iv) **Maximum forward current** : The maximum current that a forward biased diode can withstand before burning out or being seriously degraded, due to high junction temperature is called maximum forward current. It is denoted as I_F (max).

v) **Peak inverse voltage** : The maximum voltage applied to the diode in the reverse direction without breakdown of the diode is called peak inverse voltage of a diode. It is also called PIV rating of a diode.

vi) **Maximum power rating** : The maximum power that the diode can dissipate safely, without increasing the junction temperature above its limiting value is called maximum power rating (MPR) of a diode. It is measured in watts.

vii) **Forward voltage drop** : It is the maximum forward voltage drop specified at certain forward current and temperature. It is denoted as V_F.

Memory Map



END...

2 Bipolar Junction Transistors and its Biasing

2.1 : Bipolar Junction Transistor

Q.1 What is transistor ?

Ans. : • Transistor is a three terminal device : Base, emitter and collector, can be operated in three configurations common base, common emitter and common collector.

• According to configuration it can be used for voltage as well as current amplification.

Q.2 Explain the word transistor.

Ans. : • The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name TRANSfer-resISTOR (TRANSISTOR).

Q.3 State the two types of transistors.

Ans. : There are two types of transistors : **Unipolar junction transistor** and **Bipolar junction transistor**.

Q.4 Why transistor is also called bipolar junction transistor ?

Ans. : The current conduction in bipolar transistor is because of both the types of charge carriers, holes and electrons. Hence this is called **Bipolar junction transistor**.

Q.5 What are the types of BJT ?

Ans. : 1. n-p-n type 2. p-n-p type

Q.6 Explain the construction of npn and pnp transistor.

Ans. : • When a transistor is formed by sandwiching a ... p-region between two n-regions, as shown in the Fig. Q.6.1 (a) ... an n-p-n type transistor. The p-n-p type transistor has a ... n-region between two p-regions, as shown in Fig. Q.6.1 (b).

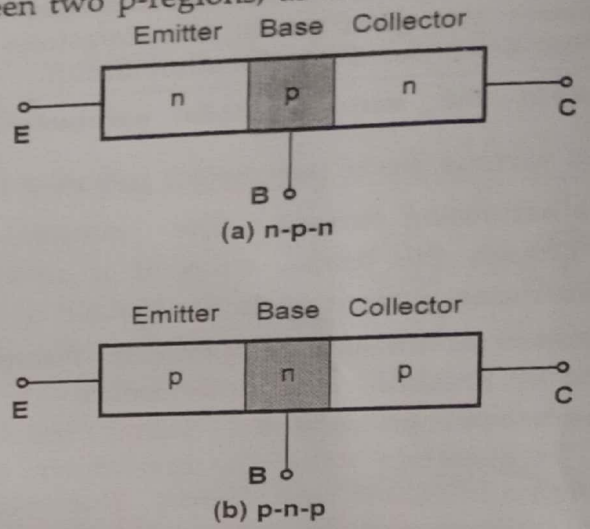


Fig. Q.6.1 Bipolar transistor construction

• The middle region of each transistor type is called the **base** ... transistor. This region is very thin and lightly doped.

• The process by which impurities are added to a semiconductor is called **doping**.

• The remaining two regions are called **emitter** and **collector**.

• The emitter and collector are **heavily** doped. But the doping in emitter is slightly greater than that of collector.

• The collector region-area is slightly more than that of emitter.

Q.7 Draw the symbols of pnp and npn transistors.

Ans. : • Fig. Q.7.1 (a) and (b) shows the symbols of npn and ... transistors. Arrow head on a transistor symbol indicates ... conventional current which is opposite to the direction of ele... current in emitter.

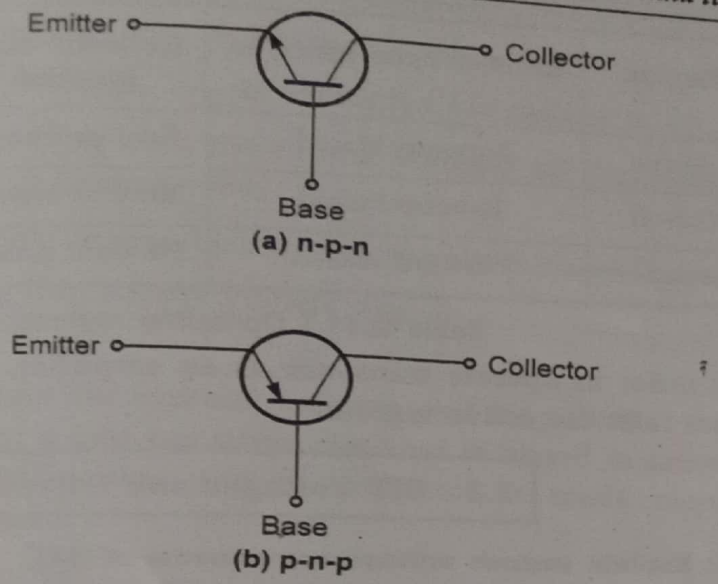


Fig. Q.7.1 Standard transistor symbols

Q.8 State the two junctions in the transistor.

Ans. : • A transistor has two p-n junctions.

• One junction is between the emitter and the base and is called the **emitter-base junction** or simply the **emitter junction** J_E.

• The other junction is between the base and the collector and is called **collector-base junction** or simply **collector junction** J_C.

2.2 : BJT Operation

Q.9 Explain the working principle of npn transistor.

Ans. : • The base to emitter junction is forward biased by the d.c. source V_{EE}. Thus, the width of depletion region at this junction is small. The collector to base junction is reverse biased and hence width of depletion region at this junction is large, shown in Fig. Q.9.1 (Fig. Q.9.1 shows conventional currents).

• The forward biased EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter

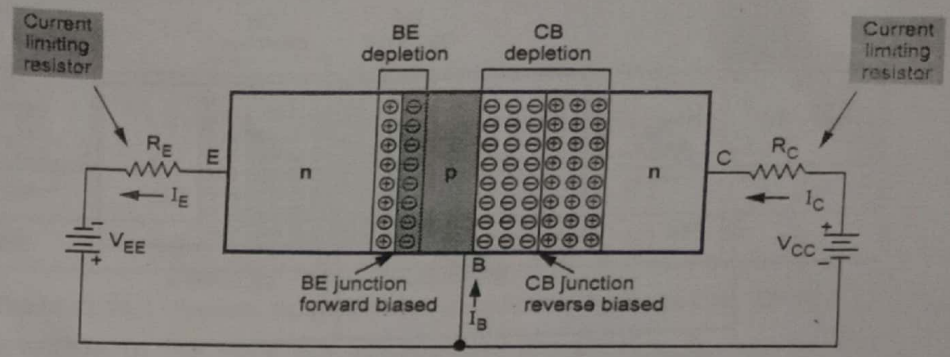


Fig. Q.9.1 Forward biased EB junction and reverse biased CB junction in npn transistor

current I_E. As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).

• Due to light doping, very few of the electrons injected into the base from the emitter recombine with holes to constitute base current, I_B and the remaining large number of electrons cross the base region and move through the collector region to the positive terminal of the external d.c. source. This constitutes collector current I_C. Thus the electron flow constitutes the dominant current in an npn transistor.

• Since, the most of the electrons from emitter flow in the collector circuit and very few combine with holes in the base. Thus, the collector current is larger than the base current.

• The emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

Q.10 Explain the working principle of pnp transistor.

Ans. : • The pnp transistor has its bias voltages V_{EE} and V_{CC} reversed from those in the npn transistor, shown in Fig. Q.10.1 (Fig. Q.10.1 shows conventional currents). This is necessary to forward-bias the emitter-base junction and reverse-bias the collector base junction in pnp transistor.

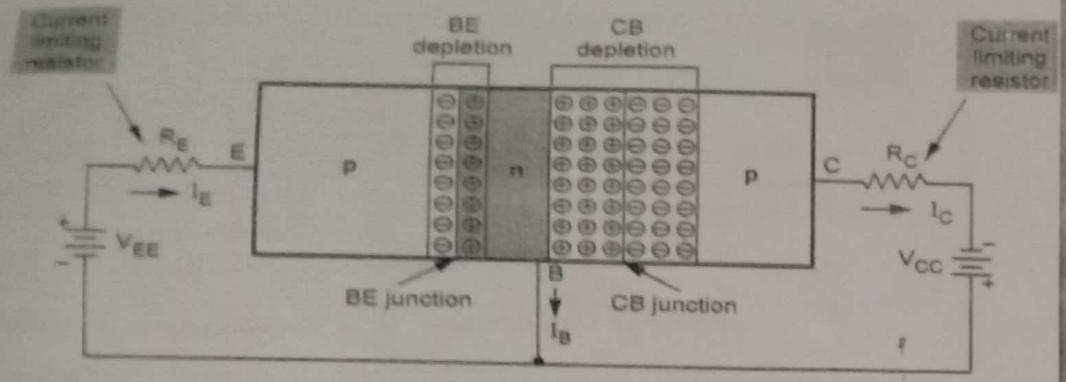


Fig. Q.10.1 Forward biased EB junction and reverse biased CB junction in pnp transistor

- The forward biased EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes flow through the n-type base, they tend to combine with electrons in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with electrons to constitute base current, I_B.
- The remaining large number of holes cross the depletion region and move through the collector region to the negative terminal of the external dc source. This constitutes collector current I_C. Thus the hole flow constitutes the dominant current in an pnp transistor.
- Like npn transistor, in pnp transistor the emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

Q.11 State the operating regions of BJT.

Ans. : • Depending upon external bias voltage polarities used, the transistor works in one of the three regions : 1) **Active region** 2) **Cut-off region** and 3) **Saturation region.**

Region	Emitter-base junction	Collector-base junction	Application
Active	Forward biased	Reverse biased	Amplifier
Cut-off	Reverse biased	Reverse biased	Off-Switch
Saturation	Forward biased	Forward biased	On-Switch

Table Q.11.1 Operating regions

- **In order to operate transistor as an amplifier, it is necessary to bias it in the active region.**

2.3 : BJT Voltages and Current

Q.12 Explain various voltage components of BJT.

Ans. : • Fig. Q.12.1 shows the terminal voltages and its polarity for an npn transistor. The voltage between base and emitter is denoted as V_{BE}. For V_{BE}, base is positive than emitter because in npn transistor, the base is biased positive with respect to the emitter.

- The voltage between the collector and the emitter is denoted as V_{CE} and the voltage between the collector and the base is denoted as V_{CB}. Since collector is positive with respect to base and emitter the polarities are as shown in the Fig. Q.12.1.

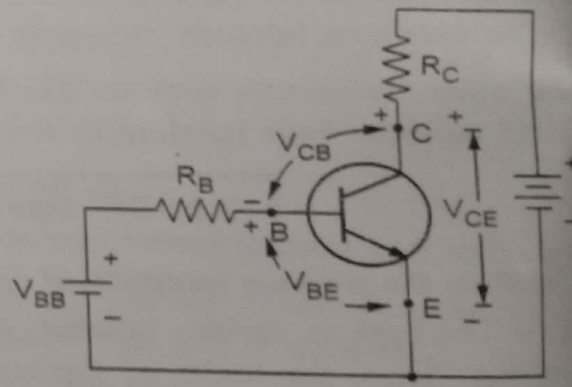


Fig. Q.12.1 Voltage source connection for npn transistor

- Fig. Q.12.1 shows the npn transistor with voltage source connections. The voltage sources are connected to the transistor with series resistors. These resistors are called **current limiting resistors.**

- The base supply voltage V_{BB} is connected via resistor R_B, and the collector supply voltage, V_{CC} is connected via resistor R_C.
- The negative terminals of both the supply voltages are connected to emitter terminal of the transistor.
- To make CB junction reverse biased, the supply voltage V_{CC} is always much larger than supply voltage V_{BB}.

pnp Transistor

- The Fig. Q.12.2 shows the terminal voltages and its polarities for a pnp transistor. For a pnp transistor, the base is biased negative with respect to the emitter, and the collector is made more negative than the base.
- Fig. Q.12.2 shows the pnp transistor with voltage source connections. Like npn transistor voltage sources are connected with series resistors. The source voltage positive terminals are connected at the emitter with V_{CC} larger than V_{BB} to keep collector-base junction reverse biased.

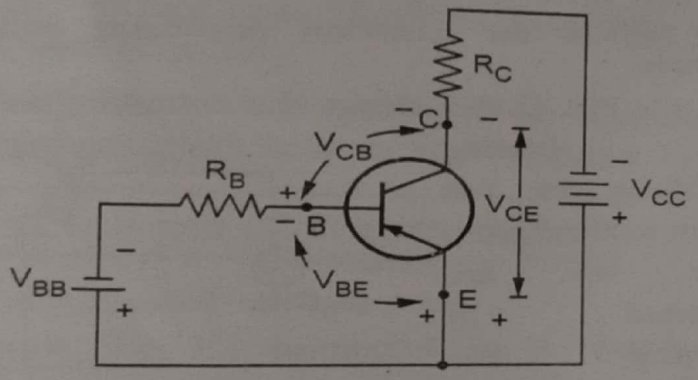


Fig. Q.12.2 Voltage source connection for pnp transistor

Q.13 State the junction voltages of BJT.

Ans. : • In different conditions such as active, saturation and cutoff there are different junction voltages. The junction voltages for a typical npn transistor at 25 °C are given in the Table Q.13.1.

Type	$V_{CE\ sat}$	$V_{BE\ sat}$	$V_{BE\ active}$	$V_{BE\ cutin}$	$V_{BE\ cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	– 0.1

Table Q.13.1 Typical npn transistor junction voltages at 25 °C

- The entries in the table are appropriate for an npn transistor. For pnp transistor the signs of all entries should be reversed.

Q.14 Explain the various current components of the transistor.

Ans. : • The directions of conventional currents in an npn transistor are as shown in Fig. Q.14.1 (a) and Fig. Q.14.1 (c) and those for a pnp are shown in Fig. Q.14.1 (b) and Q.14.1 (d). Figures show the conventional currents using the schematic symbols of npn and pnp transistors, respectively.

- It can be noticed that the arrow at the emitter of the transistor's symbol points in the direction of conventional current.
- Let us consider pnp transistor. The current flowing into the emitter terminal is referred to as the emitter current and identified as I_E. The currents flowing out of the collector and base terminals are referred to as collector current and base current, respectively. The collector current is identified as I_C and base current as I_B.

For both npn and pnp transistors.

$$I_E = I_B + I_C$$

Refer Fig. Q.14.1 on next page.

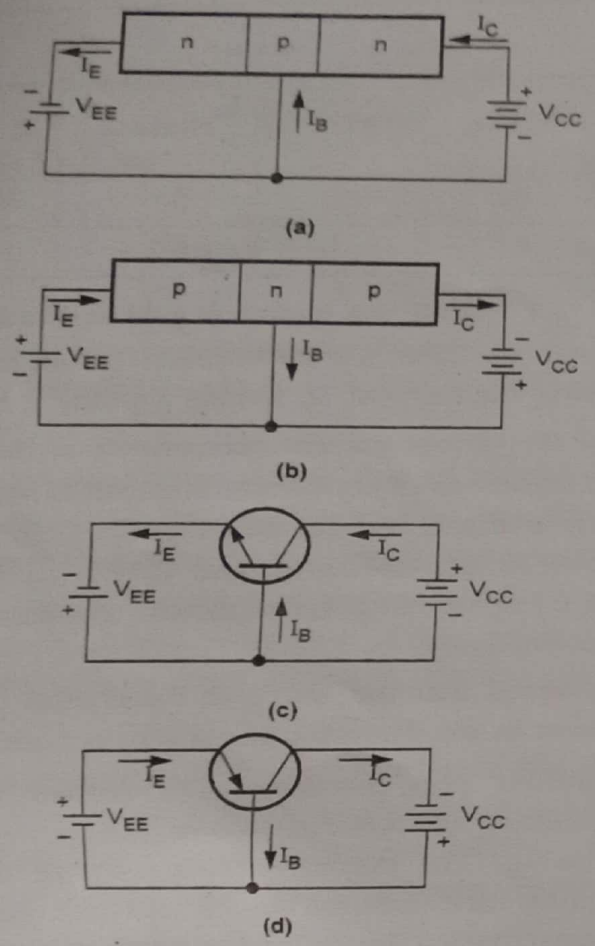
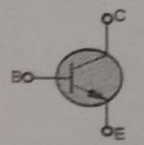
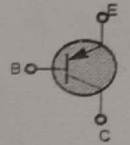


Fig. Q.14.1 Transistor conventional current directions

Q.15 Give the comparison between pnp and npn transistors.

Ans. :

Sr.No.	Parameter	npn transistor	pnp transistor
1.	Symbol		

2	Carriers	Electrons are the more important carriers	Holes are the more important carriers
3.	Voltage applied and current direction	A positive voltage is given to the collector terminal to produce a current flow from the collector to the emitter.	A positive voltage is given to the emitter terminal to produce current flow from the emitter to collector.
4.	V_{CE}	Positive	Negative
5.	Emitter arrow	Pointed out	Pointed in
6.	The current directions and voltage polarities in PNPs and NPNs are always opposite to each other.		

Q.16 Explain the transistor amplifying action with the help of example.

Ans. : • Fig. Q.16.1 shows the common-base amplifier circuit. The dc biasing conditions are not shown in the figure. Since we are interested in analysing a.c. response.

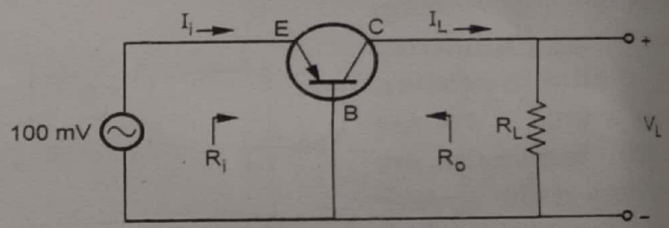


Fig. Q.16.1 CB amplifier

- For CB configuration the a.c. input resistance (R_i) is quite small typically varies from 10 Ω to 100 Ω.
- On the other hand, a.c. output resistance (R_o) for CB configuration is quite high. It varies from 50 K to 1 MΩ.
- The difference in resistance is due to the forward-biased junction at the input (BE junction) and the reverse-biased junction at the output (BC junction).
- If we assume R_i = 50 Ω and R_o = 200 K we have,

$$I_C \approx \frac{V_R}{R_C} \approx \frac{100\ mV}{50} \approx 2\ mA$$

- If we assume $\alpha \rightarrow 1$ ($I_C \approx I_E$)

$$I_C \approx I_E \quad \text{and} \quad \therefore I_C \approx 2\ mA$$

- Assuming $R_L = 5\ K$ we have

$$R = 200\ K \parallel 5\ K = 4.878\ K$$

- The output voltage,

$$V_L = I_C \times R = 2\ mA \times 4.878\ K = 9.756\ V$$

- The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{9.756\ V}{100\ mV} = 97.56$$

- Typical values of voltage amplification provided by CB configuration vary from 50 to 300.
- The basic amplifying action was produced by transferring a current I from a low-resistance circuit to high-resistance circuit.

2.4 : CE, CB and CC Characteristics

Q.17 State the various transistor configurations.

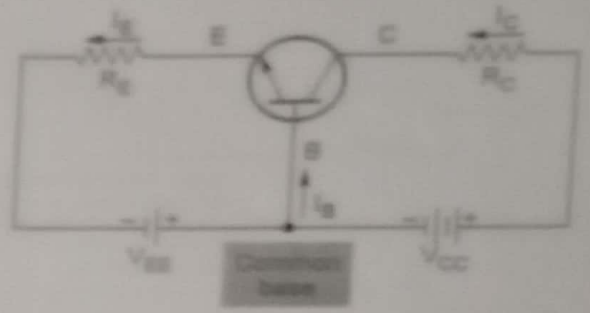
Ans. : • The transistor can be connected in a circuit in the following three configurations.

- Common base configuration
- Common emitter configuration
- Common collector configuration

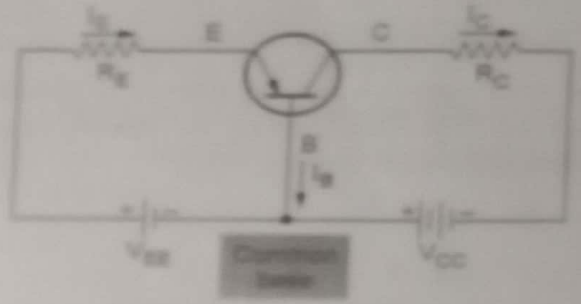
Q.18 Draw the neat circuit configuration of CB connection.

Ans. : • The Fig. Q.18.1 shows the common base configuration.

- As shown in Fig. Q.18.1, in this configuration input is applied between emitter and base and output is taken from the collector and base.
- Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.



(a) npn



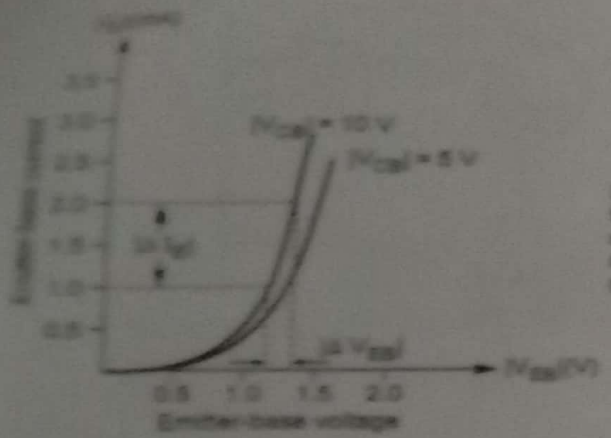
(b) pnp

Fig. Q.18.1 Common base configuration

Q.19 Draw and explain the input characteristics of CB configuration.

Ans. : • It is the curve between input voltage V_{EB} (emitter-base voltage) and input current I_E (emitter current) at constant collector-base voltage V_{CB}. The emitter current is taken along Y-axis and emitter base voltage along X-axis. Fig. Q.19.1 shows the input characteristics of a typical transistor in common-base configuration.

- From this characteristics we can observe the following important points :



Note : While plotting input characteristics the magnitudes of voltage and current are considered. Practically the voltage and current polarities are opposite for pnp and npn transistors

Fig. Q.19.1 Input characteristics of transistor in CB configuration

1. The input resistance is a ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}).

   It is given by

$$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

2. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for germanium), the emitter current (I_E) increases rapidly with small increase in emitter-base voltage (V_{EB}). Thus, the input resistance is very small.

3. It can be observed that there is slight increase in emitter current (I_E) with increase in V_{CB}. This is due to change in the width of the depletion region in the base region under the reverse biased condition.

Q.20 Define $I_{C(INJ)}$ and I_{CBO}.

Ans. : In common base configuration, the collector current I_C is given by,

$$I_C = I_{C(INJ)} + I_{CBO}$$

$I_{C(INJ)}$: It is an injected collector current due to number of electrons crossing the collector base junction.

I_{CBO} : It is the reverse saturation current flowing due to the minority carrier between collector and base when the emitter is open. I_{CBO} is negligible compared to $I_{C(INJ)}$ and therefore we have

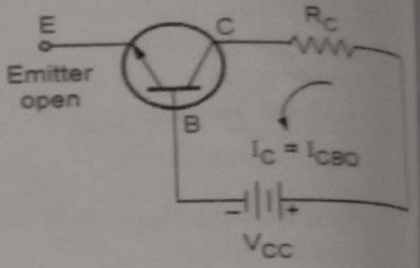


Fig. Q.20.1 CB configuration with base open

$$I_C \approx I_{C(INJ)}$$

However, when emitter is open

$$I_C = I_{CBO}$$

I_{CBO} → Collector to base leakage current

→ Emitter open

***Key Point** : The reverse saturation current, I_{CBO}, is temperature sensitive and it doubles for every 10 °C rise in temperature.*

Q.21 Define current amplification factor or current gain (α_{dc}).

Ans. : It is defined as the ratio of the collector current resulting from carrier injection to the total emitter current.

$$\therefore \quad \alpha_{dc} = \alpha \approx \frac{I_{C(INJ)}}{I_E} = \frac{I_C}{I_E}$$

$\because I_{CBO}$ is negligibly small

Since $I_C < I_E$ the value of α_{dc} is always less than unity. It ranges from 0.95 to 0.995 depending on the thickness of the base region. **larger the thickness of the base, smaller is the value of α_{dc}**

Q.22 What is early effect ? How can it account for the CB output characteristics ?

Ans. : • When reverse bias voltage V_{CB} increases, the width of depletion region also increases, which reduces the electrical base width. This effect is called as **'Early effect'** or **'Base width modulation'**.

• This decrease in base width has two consequences.

1. There is less chance for recombination within the base region. Hence the transport factor β^*, and also α, increase with an increase in the magnitude of the collector junction voltage.
2. The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the junction increases. This increases emitter current slightly. Refer Fig. Q.22.1.

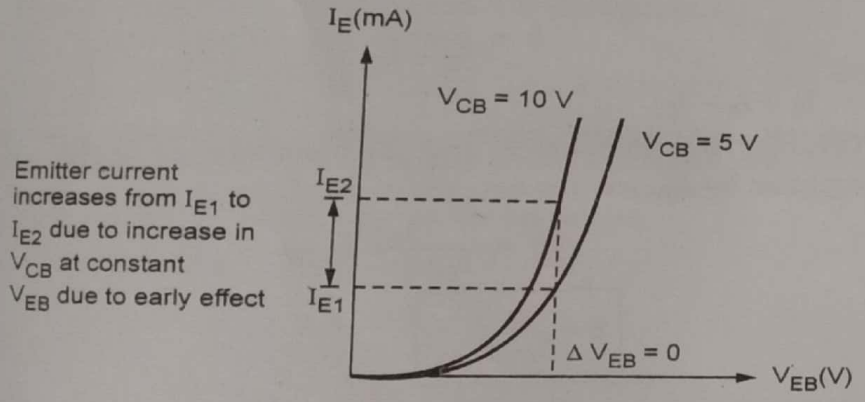
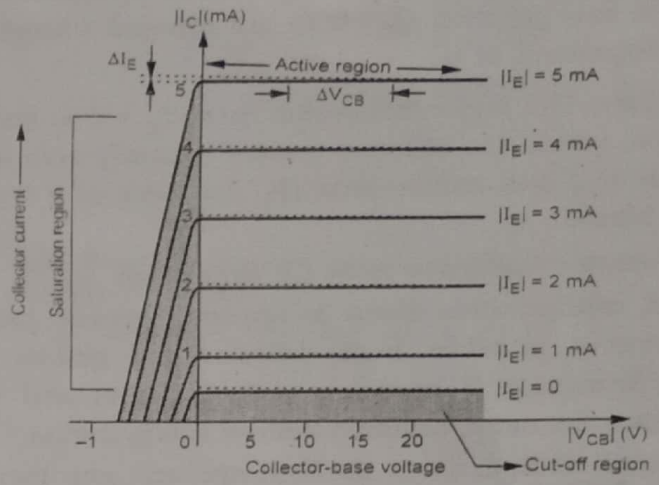


Fig. Q.22.1

Q.23 Draw and explain the output characteristics of CB configuration.

Ans. : • It is the curve between collector current I_C and collector base voltage V_{CB} at constant emitter current I_E. The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis. Fig. Q.23.1 shows the output characteristics of a typical transistor in common base configuration.

From this characteristics we observe following points :



Note : While plotting output characteristics the magnitudes of voltage and current are considered. Practically the voltage and current polarities are opposite for pnp and npn transistors

Fig. Q.23.1 CB output characteristics

1. The output characteristics has three basic regions : **Active**, **cut-off** and **saturation**.
2. **Active region :**
   - For the operation in the active region, the emitter-base junction (J_E) is **forward biased** while collector base junction (J_C) is **reverse biased**.
   - In this region, collector current I_C is approximately equal to the emitter current (I_E) and transistor works as an amplifier.
   - In the active region, the collector current is essentially almost constant.
   - The Dynamic output resistance is the ratio of change in collector base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E). It is given by

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{Constant}}$$

   - The collector current I_C is almost independent on collector-base voltage V_{CB} and the transistor can be said to work as constant-current source. This provides very high dynamic output resistance.

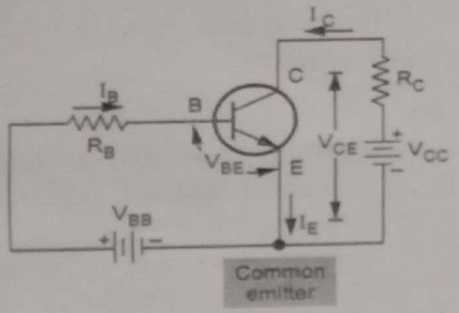
3. **Saturation region** : In this region, the emitter-base junction (J_E) and collector base junction (J_C) both are **forward biased**. Here, the I_C is independent of I_B.

4. **Cut-off region** : The region below the curve $I_E = 0$ is known as cut-off region, where the collector current is nearly zero and the collector-base (J_C) and emitter-base (J_E) junctions of a transistor are **reverse biased**.

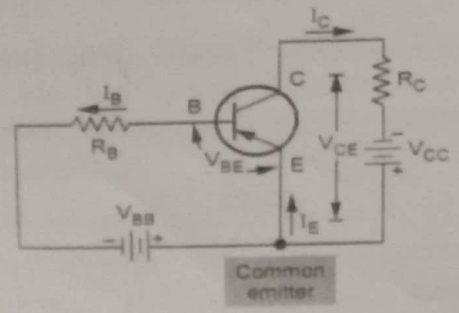
Q.24 Draw the circuit configuration of CE connection.

Ans. : • In this configuration input is applied between base and emitter, and output is taken from collector and emitter. Here, emitter of the transistor is common to both, input and output circuits, and hence the name common emitter configuration.

• Common emitter configurations for both npn and pnp transistors are shown in Fig. Q.24.1 (a) and Q.24.1 (b), respectively.



(a) npn



(b) pnp

Fig. Q.24.1 Common emitter configurations

Q.25 Define β_{dc}.

Ans. : • The β_{dc} is the ratio of output current I_C and input current I_B in common emitter configuration. It is **common emitter amplification factor** or **current gain**.

• It is given by,

$$\beta_{dc} = \frac{I_C}{I_B}$$

Q.26 Derive the relationship between α_{dc} and β_{dc}.

Ans. :

$$\beta = \frac{I_C}{I_B}$$

We have, $I_E = I_C + I_B$ i.e. $I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

$\because$ $I_B = I_E - I_C$

Dividing the numerator and denominator of R.H.S. of above equation by I_E, we get,

$$\beta = \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1 - \alpha}} \qquad \because \alpha = \frac{I_C}{I_E}$$

We know that, $\alpha = \frac{I_C}{I_E}$ and $I_E = I_B + I_C$

$$\alpha = \frac{I_C}{I_B + I_C}$$

Dividing the numerator and denominator of R.H.S. of above equation by I_B, we get,

$$\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$$

$$\therefore \quad \boxed{\alpha = \frac{\beta}{1 + \beta}} \qquad \because \beta = \frac{I_C}{I_B}$$

Q.27 Calculate the values of I_C and I_E for a BJT with α_{dc} = 0.97 and I_B = 50 μA. Determine β_{dc} for the device.

Ans. :

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.97}{1-0.97} = 32.33$$

$$I_C = \beta I_B = 32.33 \times 50\ \mu A = 1.6165\ mA$$

$$I_E = I_B + I_C = 50\ \mu A + 1.6165\ mA = 1.6665\ mA$$

Q.28 Define reverse leakage current (I_{CEO}) in CE configuration.

Ans. : In CE configuration,

$$\boxed{I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}} \quad \ldots (1)$$

The terms $(1 + \beta_{dc}) I_{CBO}$ in equation (1) is denoted as I_{CEO} and is the reverse saturation current for the CE configuration.

$$\therefore \quad \boxed{I_C = \beta_{dc} I_B + I_{CEO}} \qquad \because (1+\beta_{dc}) I_{CBO} = I_{CEO}$$

Q.29 For a transistor in common emitter configuration, the reverse leakage current is 21 μA, whereas when the same transistor is connected in common base configuration, it reduces to 1.1 μA. Calculate values of α_{dc} and β_{dc} of the transistor.

Ans. : Given : I_{CBO} = 1.1 μA, I_{CEO} = 21 μA

$$I_{CEO} = (1 + \beta_{dc})\ I_{CBO}$$

$$\therefore \quad 1 + \beta_{dc} = \frac{I_{CEO}}{I_{CBO}} = \frac{21\ \mu A}{1.1\ \mu A} = 19.09$$

$$\therefore \quad \beta_{dc} = 18.09$$

$$\therefore \quad \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{18.09}{1+18.09} = 0.9476$$

Q.30 Calculate the α_{dc} and β_{dc} for the given transistor for which I_C = 5 mA, I_B = 50 μA and I_{CO} = 1 μA.

Ans. :

$$I_C = 5\ mA, \quad I_B = 50\ \mu A, \quad I_{CO} = I_{CBO} = 1\ \mu A$$

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}$$

$$\therefore \quad 5 \times 10^{-3} = \beta_{dc} \times 50 \times 10^{-6} + (1+\beta_{dc}) \times 1 \times 10^{-6}$$

$$\therefore \quad 5 \times 10^{-3} - 1 \times 10^{-6} = 51 \times 10^{-6}\ \beta_{dc}$$

$$\therefore \quad \beta_{dc} = \frac{4.999 \times 10^{-3}}{51 \times 10^{-6}} = 98$$

$$\therefore \quad \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{98}{1+98} = 0.9899$$

Q.31 The BJT circuit has I_E = 10 mA and α = 0.98. Determine the value of β and I_C.

Ans. : Given : I_E = 10 mA and α = 0.98

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_E = \frac{(1+\beta) I_C}{\beta} = 10.2\ mA$$

Q.32 Draw and explain the input characteristics of transistor in CE mode.

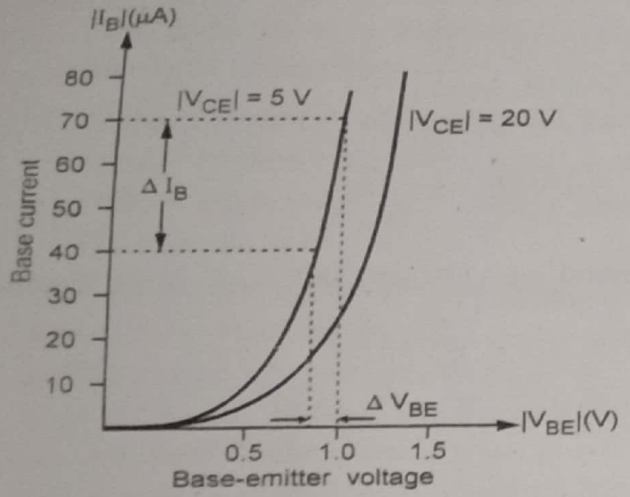
Ans. : • The input voltage in the CE configuration is the base-emitter voltage and the output voltage is the collector-emitter voltage. The input current is I_B and the output current is I_C.

• Input characteristics is the curve between input voltage V_{BE} (base-emitter voltage) and input current I_B (base current) at constant collector-emitter voltage, V_{CE}. The base current is taken along Y-axis and base emitter voltage V_{BE} is taken along X-axis. Fig. Q.32.1 shows the input characteristics of a typical transistor in common-emitter configuration.

From this characteristics we observe the following important points :

1. The input resistance is the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector emitter voltage V_{CE}. It is given by,

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}\Big|_{V_{CE}=\text{Constant}}$$



Note : While plotting input characteristics the magnitudes of voltage and current are considered Practically the voltage and current polarities are opposite for pnp and npn transistors

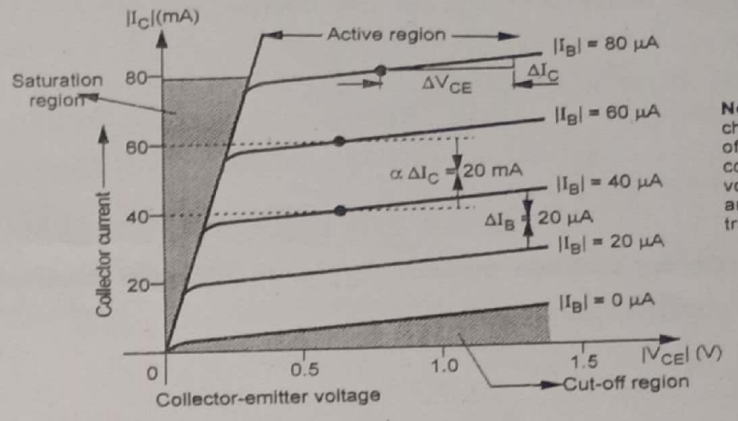
Fig. Q.32.1 Input characteristics of the transistor in CE configuration

2. After the cut-in voltage, the base current (I_B) increases rapidly with small increase in base-emitter voltage (V_{BE}). Thus the dynamic input resistance is small in CE configuration.
3. For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased.

Q.33 With a neat diagram explain the output characteristics of npn transistor in CE configuration.

Ans. : 1. This characteristics shows the relation between the collector current I_C and collector voltage V_{CE}, for various fixed values of I_B. This characteristics is often called collector characteristics. A typical family of output characteristics for an n-p-n transistor in CE configuration is shown in Fig. Q.33.1.

2. The value of β_{dc} of the transistor can be found at any point on the characteristics by taking the ratio I_C to I_B at that point, i.e. $\beta_{dc} = I_C / I_B$. This is known as D.C. beta for the transistor.



Note : While plotting output characteristics the magnitudes of voltage and current are considered. Practically the voltage and current polarities are opposite for pnp and npn transistors

Fig. Q.33.1 Output characteristics of the transistor in CE configurat

3. From the output characteristics, we can see that change collector-emitter voltage (ΔV_{CE}) causes the little change in collector current (ΔI_C) for constant base current I_B. Thus output dynamic resistance is high in CE configuration.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{Constant OR } \Delta I_B = 0}$$

- The output characteristics of common emitter configura consists of three regions : **Active, Saturation** and **Cut-off**.

Active Region :

- For the operation in the active region, the emitter-b junction (J_E) is **forward biased** while collector base junct (J_C) is **reverse biased**.
- The collector current rise more sharply with increasing V_{CE} the linear region of output characteristics of CE transistor.

Saturation region :

- In this region, the emitter-base junction (J_E) and collector b junction (J_C) both are **forward biased**.

- The saturation value of V_{CE}, designated $V_{CE\,(sat)}$, usually ranges between 0.1 V to 0.3 V.

Cut-off region :

- The region below $I_B = 0$ is the cut-off region of operation for the transistor. In this region, both the junctions of the transistor are reverse biased.

To identify the operating region of transistor we can observe certain conditions. These are :

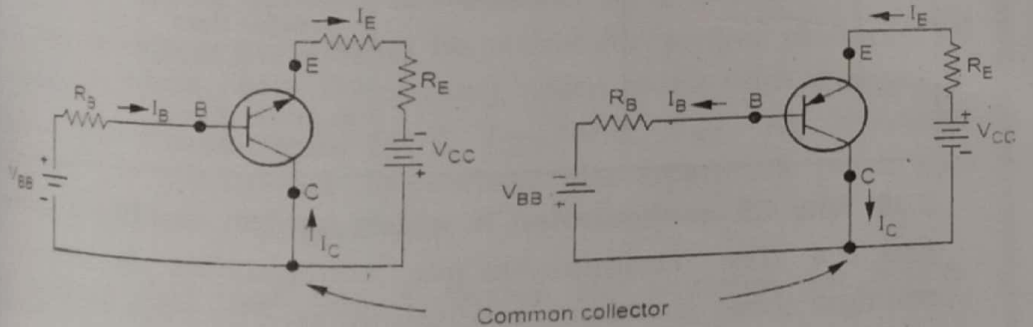
For saturation : $I_B > \frac{I_C}{\beta_{dc}}$ **For cut-off :** $I_B = 0$

For active region : $V_{CE} > V_{CE\,(sat)}$

Q.34 Draw the neat circuit configuration of CC.

Ans. : • The Fig. Q.34.1 shows the common collector configuration. In this configuration, input is applied between base and collector and output is taken from emitter and collector.

- Here, collector of the transistor is common to both input and output circuits and hence the name common collector configuration.
- Common collector connections for both npn and pnp transistors are shown in Fig. Q.34.1 (a) and Q.34.1 (b), respectively.



(a) npn (b) pnp

Fig. Q.34.1 Common collector configurations

- Here, the output at the emitter follows the input at the base and hence this configuration is also known as **emitter follower** configuration.

Q.35 Sketch and explain the input characteristics of transistor in CC configuration.

Ans. : • The input characteristics of CC configuration is a graph of input current I_B (base current) versus input voltage V_{CB} (collector base voltage) at constant V_{CE}. The base current is taken along Y-axis and collector base voltage V_{CB} is taken along X-axis.

- Fig. Q.35.1 shows the input characteristics of a typical transistor in common-collector configuration.

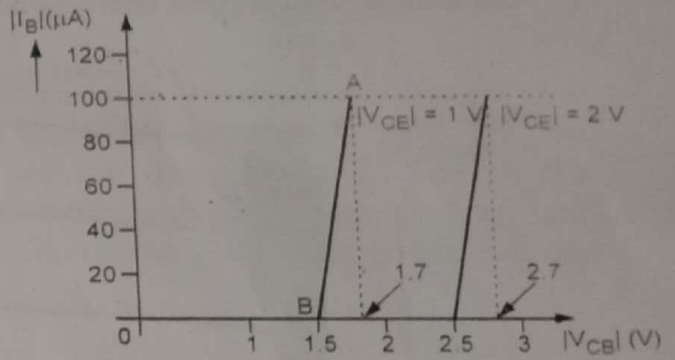


Fig. Q.35.1 Input characteristics of transistor in CC configuration

- The common collector input characteristics are quite different from either common base or common emitter input characteristics.
- This difference is due to the fact that the input voltage V_{CB} is largely determined by the level of collector to emitter voltage V_{CE}.
- Looking at Fig. Q.35.1 we can write,

$$V_{CE} = V_{CB} - V_{BE}$$

or

$$V_{CB} = V_{CE} + V_{BE}$$

- In CC configuration input junction is BC and it is reversed biased so input resistance in CC configuration is very high.

Q.36 Sketch and explain the output characteristics of transistor in CC configuration.

Ans. : • *It is the curve between emitter current* I_E *and collector to emitter voltage* V_{CE} *at constant base current* I_B. *The emitter current is taken along Y–axis and collector to emitter voltage along X–axis.*

• *Fig. Q.36.1 shows the output characteristics of a typical transistor in common collector configuration.*

• Since, I_C is approximately equal to I_E, the common collector output characteristics are practically similar to those of the common emitter output characteristics.

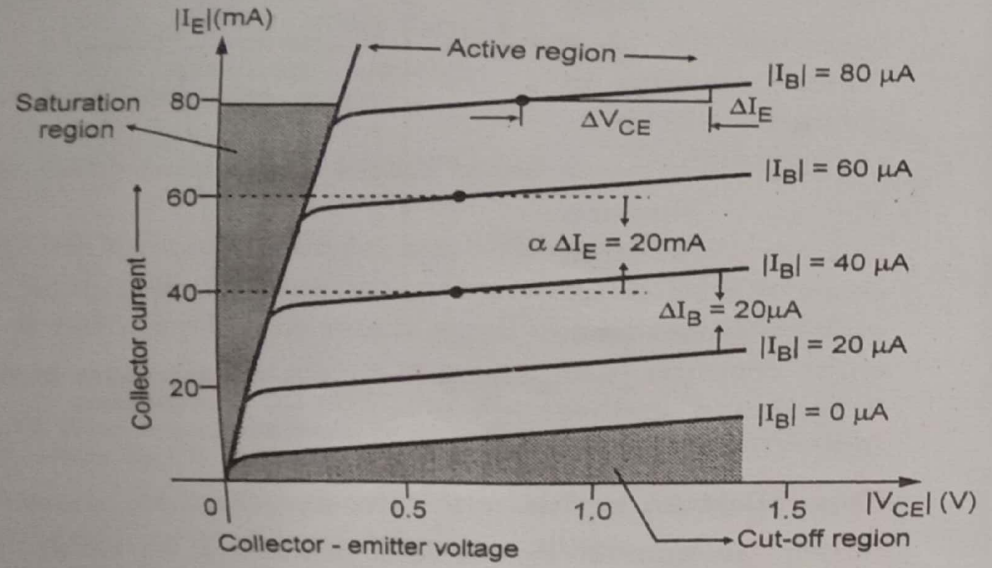


Fig. Q.36.1 Output characteristics of the transistor in CC configuration

Q.37 What is the current gain of CC configuration ?

Ans. : • The current gain of CC configuration is given by

$$\gamma = \frac{I_E}{I_B} = \frac{I_B + I_C}{I_B} = 1 + \frac{I_C}{I_B} = 1 + \beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

Q.38 Compare CB, CE and CC transistor configurations.

Ans. :

Sr. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance (R_i)	Very low (20 Ω)	Low (1kΩ)	High (500 kΩ)
2.	Output resistance (R_o)	Very high (1 M Ω)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and base	Base and emitter	Base and collector
6.	Output voltage taken between	Collector and base	Collector and emitter	Emitter and collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain (A_i)	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain (A_v)	Medium	Medium	Less than unity
10.	Applications	As a input stage of multistage amplifier	Provides both voltage and current gain greater than unity and hence it is widely used in audio signal amplification	For impedance matching

Q.39 Why CE configuration is widely used in amplifier circuits ?

Ans. : • The common-emitter configuration is widely used amongst three transistor configurations. The main reasons for its wide-spread use of this circuit arrangement are :

• The CE configuration is the only configuration which provides both voltage gain as well as current gain greater than unity.

- The power gain is a product of voltage gain and current gain. The power gain of the CE amplifier is much greater than the power gain provided by the other two configurations.
- In a common emitter circuit, the ratio of output resistance to input resistance is small, may range from 10 Ω to 100 Ω. This makes configuration an ideal for coupling between various transistor stages.

2.5 : DC Load Line and Bias Point

Q.40 Why biasing is needed in a transistor ?

Ans. : In order to operate transistor in the desired (cut-off, active or saturation) region we have to apply external d.c. voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Because d.c. voltages are used to bias the transistor, biasing is known as **d.c. biasing** of the transistor.

Q.41 Define DC operating point.

Ans. : When we bias a transistor, we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or **d.c. operating point** or **quiescent point.**

Q.42 State the factors affecting the stability of Q point.

Ans. : The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as β, I_{CO} and V_{BE}. As transistor parameters are temperature dependent, the operating point also varies with changes in temperature.

Q.43 What is d.c. load line ? Derive its equation for a CE amplifier.

Ans. : Definition : The d.c. load line is the line drawn on the output characteristics of CE amplifier considering only d.c. operating conditions and the slope of the line is $-1/R_C$ where R_C is the load resistance.

- Applying KVL to the collector circuit we have

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad \ldots (1)$$

- Rearranging the terms in above equation we get,

$$I_C = \left[-\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C} \quad \ldots (2)$$

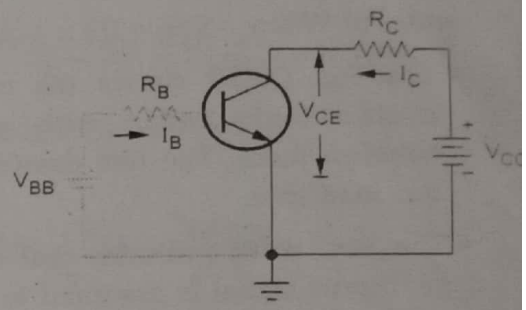


Fig. Q.43.1 Common emitter configuration

- If we compare this equation with equation of straight lin $y = mx + c$, where m is the slope of the line and c is th intercept on Y-axis, then we can draw a straight line on th graph of I_C versus V_{CE} which is having slope $-1/R_C$ an Y-intercept V_{CC}/R_C. To determine the two points on the line w assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$.

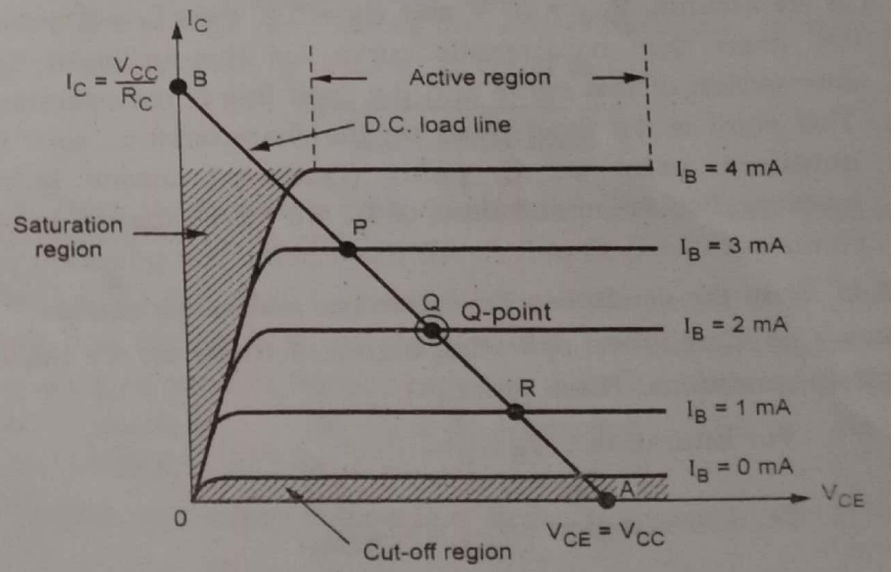


Fig. Q.43.2 Common emitter output characteristics with d.c. load

a) When $V_{CE} = V_{CC}$; $I_C = 0$ and we get a point A

and b) When $V_{CE} = 0$; $I_C = V_{CC}/R_C$ and we get a point B

- The Fig. Q.43.2 shows the output characteristics of a common emitter configuration with points A and B and line drawn between them. The line drawn between points A and B is called *d.c. load line*.

- The 'd.c.' word indicates that only d.c. conditions are considered, i.e. inputs signal is assumed to be zero.

Q.44 What is Q-point ?

Ans. : Applying Kirchhoff's voltage law to the base circuit of Fig. Q.44.1, we get,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

As $V_{BB} >> V_{BE}$, $I_B = \frac{V_{BB}}{R_B}$

- If we assume, $V_{BB} = 10$ V and $R_B = 5$ K then $I_B = 2$ mA. Now, if we draw the characteristic curve for this value of I_B ; then intersection of this curve and d.c. load line is the operating point. This point is the fixed point on the characteristics, so it is called **quiescent point** or **Q point** (Quiescent means quiet, still, inactive). For different values of I_B, we have different intersection points such as P, Q and R. All these points are quiescent points.

Q.45 State the conditions for saturation and active regions.

Ans. : To identify the operating region of transistor we can observe certain conditions. These are :

For saturation : $I_B > \frac{I_C}{\beta_{dc}}$

For active region : $V_{CE} > V_{CE\,(sat)}$

Q.46 Explain the criteria for selection of the operating point.

OR Explain the role of Q-point on d.c. load line.

Ans. : The operating point can be selected at three diffe positions on the d.c. load line : Near saturation region, near cu region or at the centre, i.e. in the active region. The selectio operating point will depend on its application. When transisto used as an amplifier, the Q-point should be selected at the ce of the d.c. load line to prevent any possible distortion in amplified output signal.

In case of switching operation, the operating point should be in saturation region for ON-operation and it should in cut-off reg for OFF-operation.

Q.47 Determine I_B , I_C , I_E , V_{CE} in the circuit of Fig. Q.47.1. The transistor has a $\beta = 150$. Assume $V_{BE} = 0.7$ V. Also draw DC load line and show Q-point.

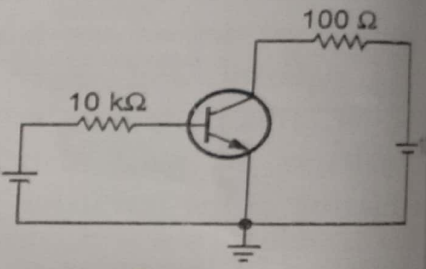


Fig. Q.47.1

Ans. : Applying KVL to the base circuit we have,

$$1.5 - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{1.5 - V_{BE}}{R_B} = \frac{1.5 - 0.7}{10 \times 10^3} = 80\ \mu A$$

$$\therefore \quad I_C = \beta I_B = 150 \times 80\ \mu A = \mathbf{12\ mA}$$

$$\therefore \quad I_E = I_B + I_C = 80\ \mu A + 12\ mA = 12.08\ mA$$

Applying KVL to the collector circuit we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C = 10 - 12 \times 10^{-3} \times 100$$

$$= 8.8\ V$$

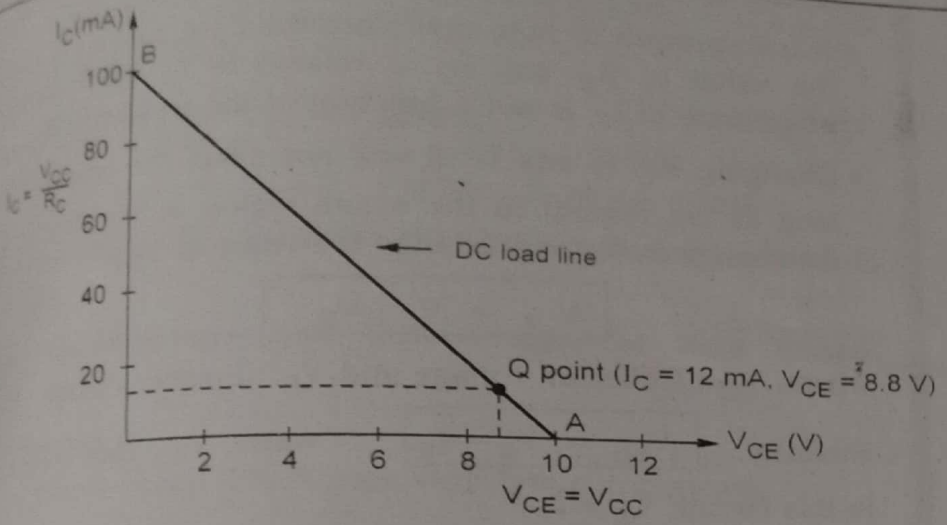


Fig. Q.47.2 DC load line

Let us find point A and point B

Point A : $V_{CE} = V_{CC} = 10$ V and $I_C = 0$

Point B : $V_{CE} = 0$ and $I_C = V_{CC}/R_C = 0.1 = 100$ mA

Q.48 Determine whether or not the transistor in Fig. Q.48.1 is in saturation. Assume $V_{CE(Sat)}$ = 0.2 V.

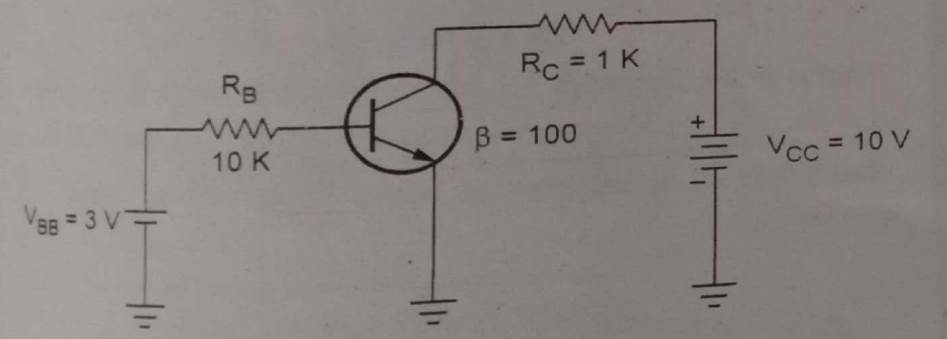


Fig. Q.48.1

Ans. : Assume transistor is in saturation. Therefore, $V_{CE(Sat)}$ = 0.2 V and $V_{BE(Sat)}$ = 0.8 V.

Applying KVL to the collector circuit we have,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10 - 0.2}{1K} = 9.8 \text{ mA}$$

Applying KVL to the base circuit we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3 - 0.8}{10 \text{ K}} = 220 \ \mu\text{A}$$

$$\frac{I_C}{\beta} = \frac{9.8 \text{ mA}}{100} = 98 \ \mu\text{A}$$

Since $I_B > \frac{I_C}{\beta}$, our assumption is true.

Q.49 Explain the effect of emitter resistor on Q point and DC load line.

Ans. : Since both the resistors R_C and R_E are present, the total dc load is $R_C + R_E$

$$\therefore \quad V_{CE(Q)} = V_{CC} - I_C(R_C + R_E)$$

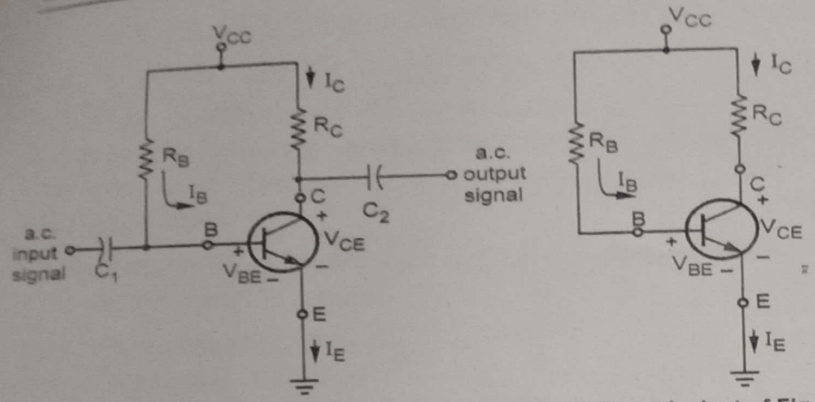
Note : The voltage drop across the emitter resistor is actually $I_E R_E$, but for convenience I_E is taken as equal to I_C.

2.6 : Base Bias

Q.50 Draw and explain the base bias circuit and device the expressions for I_B, I_C and V_{CE}.

Ans. : • The Fig. Q.50.1 shows the base bias circuit. It is also called fixed bias circuit. It is the simplest d.c. bias configuration. For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for d.c. is $X_C = 1 / 2\pi fC = 1 / 2\pi(0)C = \infty$.

• The d.c. equivalent of base bias circuit is shown in Fig. Q.50.1 (b).



(a) Base bias circuit (b) D.C. equivalent of Fig. Q.49.1 (a)

Fig. Q.50.1

Base Circuit

- Applying Kirchhoff's voltage law (KVL) to the base circuit shown in Fig. Q.50.2 we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \ldots (1)$$

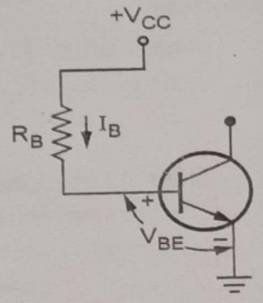


Fig. Q.50.2 Base circuit of the base bias circuit

Collector Circuit

Applying Kirchhoff's voltage law to the collector circuit shown in Fig. Q.50.3 we get,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_C R_C} \quad \ldots (2)$$

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \quad \ldots (3)$$

The magnitude of collector current is given by,

$$\therefore \quad \boxed{I_C = \beta I_B} \quad \ldots (4)$$

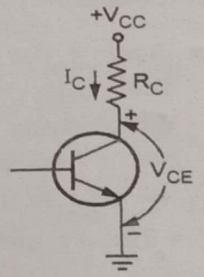


Fig. Q.50.3 Collector circuit of the base bias circuit

- It is important to note that since the base current is controlled by the value of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C.
- Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However the change in R_C will change the value of V_{CE}.

$$\boxed{V_{CE} = V_C - V_E} \quad \ldots (5)$$

where, V_C : Collector voltage and V_E : Emitter voltage

Similarly, $\boxed{V_{BE} = V_B - V_E}$ where, V_B : Base voltage ... (6)

In this circuit, $V_E = 0$,

$\therefore \quad V_{BE} = V_B$ and $V_{CE} = V_C$ ... (7)

Q.51 For the circuit shown in the Fig. Q.51.1. Calculate $I_B, I_C, V_{CE}, V_B, V_C$ and V_{BC}. Assume $V_{BE} = 0.7$ V and $\beta = 50$.

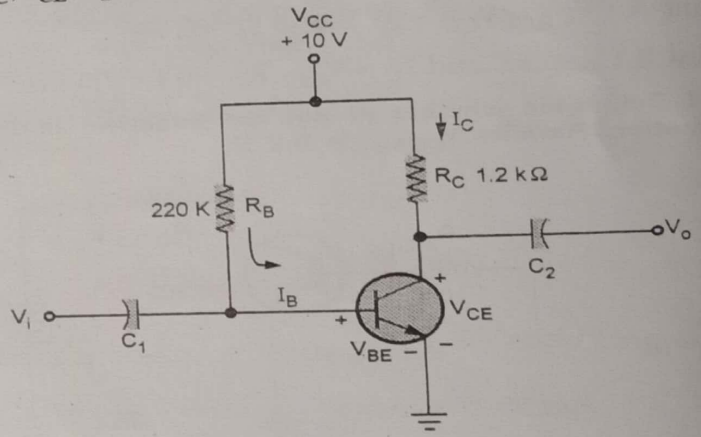


Fig. Q.51.1

Ans. : $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{10 - 0.7}{220 \times 10^3} = 42.27\ \mu A$

$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = \mathbf{2.1135\ mA}$

$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3 = 7.463$

$$V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{CE} = 7.4638 \text{ V}$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 = -6.7638$$

The negative voltage V_{BC} indicates that base-collector junction is reverse biased.

Q.52 State the advantages and disadvantages of base biased circuit.

Ans. : **Advantages :**

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages

1. This circuit does not provide any check on the collector current which increases with the rise in temperature. i.e. thermal stability is not provided by this circuit. So the operating point is not maintained.

$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C = \beta I_B$ and I_B is already fixed; I_C depends on β which changes unit to unit and shifts the operating point.

Thus stabilization of operating point is very poor in the fixed bias circuit.

2.7 : Emitter Feedback Bias

Q.53 Draw and explain the emitter feedback circuit and derive the expressions for I_B, I_C and V_{CE}.

Ans. : • To improve the stability of the biasing circuit over the fixed bias circuit, the emitter resistance is connected in the biasing

circuit. Such biasing circuit is known as **emitter feedback circuit** and it is shown in the Fig. Q.53.1.

Base Circuit : Let us consider the base circuit shown in the Fig. Q.53.2.

Applying KVL to the base circuit we get,

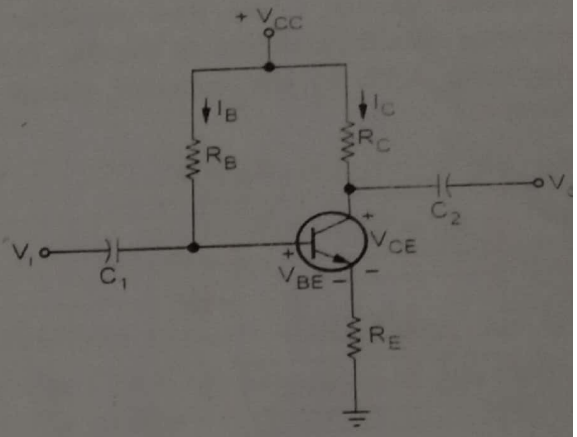


Fig. Q.53.1 Emitter feedback circuit

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E \quad \ldots(1)$$

We have, $I_E = (1+\beta) I_B$

I_E in equation (1) we get,

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\therefore V_{CC} - V_{BE} = I_B R_B + (1+\beta)\ I_B R_E$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)\, R_E}}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}} \qquad \because \beta >> 1$$

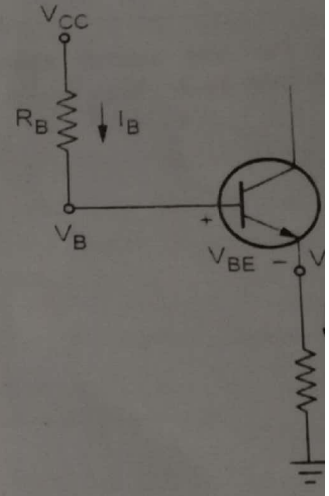


Fig. Q.53.2 Base circ

Note that the only difference between the equation for I_B and obtained for the fixed-feedback configuration is the term βR_E.

$$V_B = V_{BE} + V_E \qquad \text{or} \qquad V_{CC} - I_B R_B$$

Since $V_E = I_E R_E$

$$\boxed{V_B = V_{BE} + I_E R_E}$$

Collector Circuit : We now consider the collector circuit as shown in the Fig. Q.53.3. Applying KVL to the collector circuit we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_C = V_{CC} + I_C R_C - I_E R_E$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

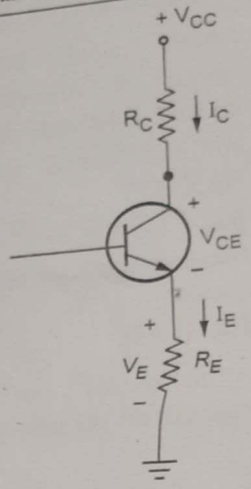


Fig. Q.53.3

Q.54 For the circuit shown in Fig. Q.54.1. Calculate I_B, I_C, V_{CE}, V_C, V_E, V_B and V_{BC}. Assume $\beta = 100$.

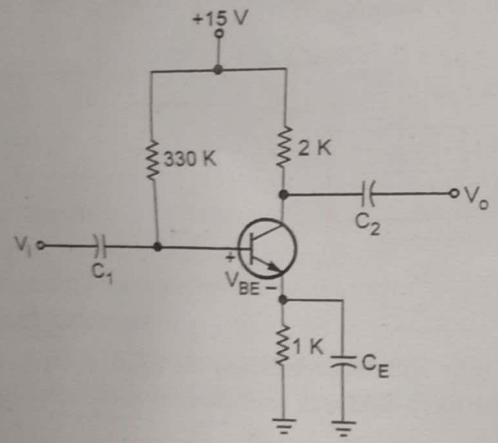


Fig. Q.54.1

Ans. :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{15 - 0.7}{330 \times 10^3 + (1+100) \times 10^3}$$

$$= 33.18\ \mu A$$

$$I_C = \beta I_B = 100 \times 33.18\ \mu A = \mathbf{3.318\ mA}$$

$$I_E = I_B + I_C = \mathbf{3.351\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 15 - 3.318 \times 10^{-3} \times 2 \times 10^3 - 3.351 \times 10^{-3} \times 1 \times 10^3$$

$$= \mathbf{5\ V}$$

$$V_C = V_{CC} - I_C R_C = 15 - 3.318 \times 10^{-3} \times 2 \times 10^3$$

$$= \mathbf{8.364\ V}$$

$$V_E = I_E R_E = 3.351 \times 10^{-3} \times 1 \times 10^3$$

$$= \mathbf{3.351\ V}$$

$$V_B = V_E + V_{BE} = 3.351 + 0.7 = \mathbf{4.051\ V}$$

$$V_{BC} = V_B - V_C = 4.051 - 8.364$$

$$= \mathbf{-4.313\ V}$$

Q.55 Determine I_{CQ} and V_{CEQ} for the network shown in Fig. Q.55.1.

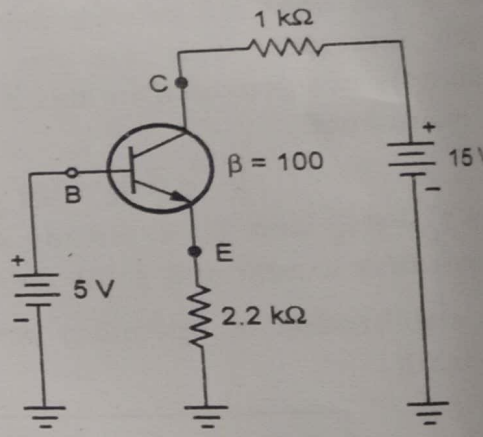


Fig. Q.55.1

Ans. : Applying KVL to the base circuit we have,

$$V_{BB} - V_{BE} - [(1+\beta) I_B \times 2.2\ K] = 0.$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{(1+\beta) \times 2.2\ K}$$

$$= \frac{5 - 0.7}{(1+100) \times 2.2\ K}$$

$$= \mathbf{19.35\ \mu A}$$

$$I_{CQ} = \beta I_B = 100 \times 19.35\ \mu A = \mathbf{1.935\ mA}$$

$$I_E = I_B + I_C = \mathbf{1.954\ mA}$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

$$= 15 - (1.935 \times 1) - (1.954 \times 2.2) = \mathbf{8.766\ V}$$

Q.56 State the advantages and disadvantages of emitter feedback circuit.

Ans. : • The addition of the emitter resistance, R_E in the emitter feedback circuit provides improved stability.

• The maximum stability is achieved when the ratio of R_B and R_E is as small as possible.

• However, when stability is increased by increasing the value of R_E, negative feedback increases which reduces the gain of the circuit.

• We can also increase stability by reducing value of R_B; however, smaller values of R_B needs separate supply voltage and adds circuit complexity.

2.8 : Collector Feedback Bias

Q.57 Explain the analysis of collector feedback configuration.

Ans. : • The Fig. Q.57.1 shows the dc bias with voltage feedback. It is also called the **collector to base bias circuit.**

• In this the biasing resistor is connected between the collector and the base of the transistor to provide a feedback path. Thus I_B flows through R_B and $(I_C + I_B)$ flows through the R_C.

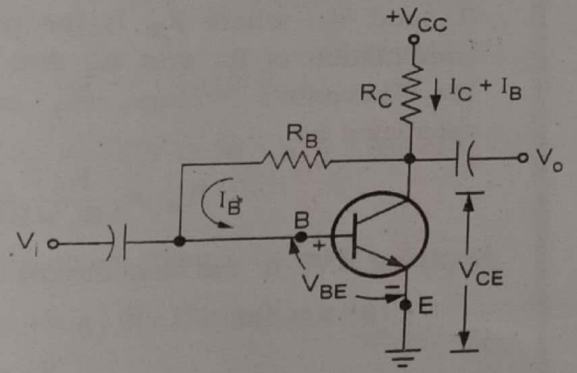


Fig. Q.57.1 D.C. bias with voltage feedback

Base Circuit

• Let us consider the base circuit of Fig. Q.57.1. Applying to the base circuit we get,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$\therefore \quad V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}} \qquad \ldots \because \beta >> 1$$

• Note that the only difference between the equation for I_B and that obtained for the fixed bias configuration is the term βR_C. Thus, we can say that the feedback path results in a reflection of the resistance R_C to the input circuit.

Collector Circuit : • Applying KVL to the collector circuit we get,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$\therefore \quad V_{CE} = V_{CC} - (I_C + I_B) R_C$$

• If there is a change in β due to piece to piece variation between transistors or if there is a change in β and I_{CO} due to the change in temperature, then collector current I_C tends to increase, since $I_C = \beta I_B + I_{CEO}$.

• As a result, voltage drop across R_C increases. Since supply voltage V_{CC} is constant, due to increase in $I_C R_C$, V_{CE} decreases. Due to reduction in V_{CE}, I_B reduces.

• As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

• In this circuit, R_B appears directly across input (base) and output (collector). A part of the output is fed back to the input, and increase in collector current decreases the base current. Thus negative feedback exists in the circuit, so this circuit is also called **voltage feedback bias circuit.**

Q.58 Calculate the Q point values (I_C and V_{CE}) for the circuit in Fig. Q.58.1.

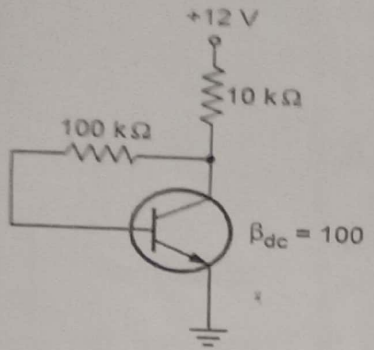


Fig. Q.58.1

Ans. : $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

$$= \frac{12 - 0.7}{100\times10^3 + (1+100)\times10\times10^3}$$

$$= 10.18\ \mu A$$

$$I_C = \beta I_B = 100 \times 10.18\ \mu A$$

$$= 1.018\ mA$$

$$V_{CE} = V_{CC} - (I_B + I_C)\ R_C$$

$$= 12 - (10.18 \times 10^{-6} + 1.018 \times 10^{-3}) \times 10 \times 10^3 = 1.7182\ V$$

2.9 : Voltage Divider Bias

Q.59 Draw the circuit diagram of voltage divider bias configuration and explain how it stabilizes operating point.

OR What is the advantage of using emitter resistance in the context of biasing ?

Ans. : • A circuit which is used to establish a stable operating point is the self-biasing circuit shown in Fig. Q.59.1.

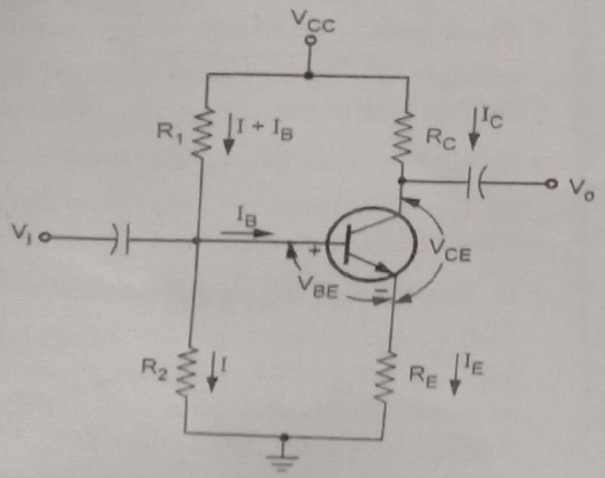


Fig. Q.59.1 Voltage divider bias circuit

- In this circuit, the biasing is provided by three resistors : R_1, R_2 and R_E.
- The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to point B which is base.
- If collector current increases due to change in temperature or change in β, the emitter current I_E also increases and the voltage drop cross R_E increases, reducing the voltage difference between base and emitter (V_{BE}).
- Due to reduction in V_{BE}, base current I_B and hence collector current I_C also reduces. Therefore, we can say that **negative feedback exists** in the voltage divider bias circuit.
- This reduction in collector current I_C compensates for the original change in I_C.
- Fig. Q.59.2 shows Thevenin's equivalent circuit of voltage divider bias. Here, R_1 and R_2 are replaced by R_B and V_T, where R_B is the parallel combination of R_1 and R_2 and V_T is the Thevenin's voltage. R_B can be calculated as

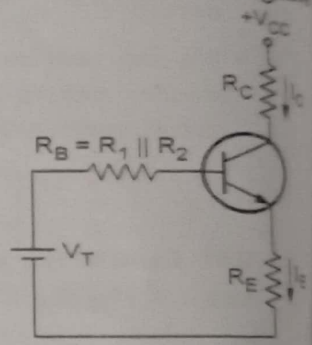


Fig. Q.59.2 Thevenin's equivalent circuit for voltage divider bias

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit of Fig. Q.59.2 we get,

$$V_T - I_B R_B - V_{BE} - (1+\beta)\ I_B\ R_E = 0$$

$$\therefore \quad I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)\ R_E}$$

Applying KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Q.60 For the circuit shown in Fig. Q.60.1, β = 100 for the silicon transistor. Calculate V_{CE} and I_C.

Ans. :

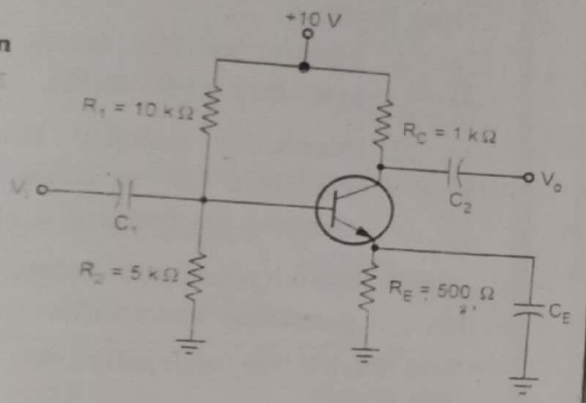


Fig. Q.60.1

$$V_T = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10$$

$$= 3.33 \text{ V}$$

$$R_B = \frac{10 \times 5}{10 + 5} = 3.33 \text{ k}\Omega$$

Applying KVL to the base circuit we get,

$$V_T - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\therefore I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{3.33 - 0.7}{3.33 \times 10^3 + (101) 500} = 48.86 \ \mu\text{A}$$

$$I_C = \beta I_B = 100 \times 48.86 \ \mu\text{A} = 4.886 \text{ mA}$$

$$I_E = 4.935 \text{ mA}$$

Applying KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 10 - 4.886 \times 1 - 4.935 \times 0.5$$

$$= 2.6465 \text{ V}$$

Q.61 State advantages and disadvantages of voltage divider bias configuration.

Ans. : • Voltage divider bias circuit provides excellent stabilization against variations in temperature and transistor gain (β).

• The negative feedback introduced by existence of R_E reduces as gain; however, this problem can be solved by using capacitor C_E

in parallel with R_E. The capacitor C_E acts as a short circuit for ac inputs and makes ac feedback equal to zero.

Q.62 Give the comparison between basic biasing circuits.

Ans. :

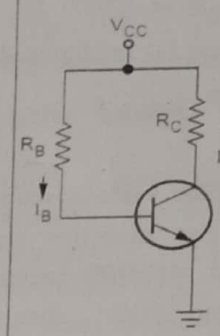
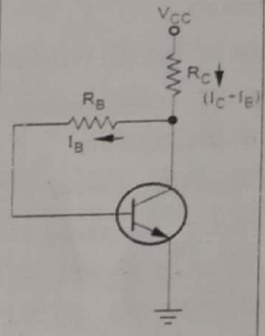
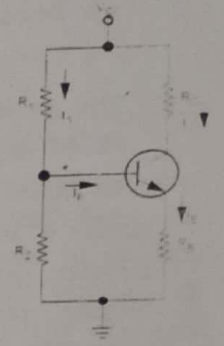
Parameter	Base bias	Collector to base bias	Voltage divider bias
Circuit			
Stability provided	Less	Medium	Highest
Feedback	No	Voltage shunt negative feedback	Current series negative feedback
Applications	Used in circuits where stability is not the important criteria	Voltage shunt feedback from the collector prevents. It is used in switching circuits.	It is most preferred biasing circuit the transistor from going into saturation. It is used in circuits where stability requirements are moderate.

Table Q.62.1 Comparison of basic biasing circuits

2.10 : Thermal Stability

Q.63 What is bias stabilization ?

Ans. : • Ideally, the Q point should be stable; it should not shift up and down on the dc load line. However, it is quite unstable.

• Two important factors are responsible for shifting the operating point are :

- Temperature
- Variation of h_{FE} (β) within manufacturers tolerance

• The process of stabilization of Q-point using biasing circuit is called **bias stabilization**.

Q.64 What is stability factor ? Define various stability factors.

Ans. : • In order to compare the stability provided by these circuits, one term is raised called **stability factor**, which indicates degree of change in operating point due to variation in temperature. Since there are three variables which are temperature dependent, we can define three stability factors as below :

i) $S_{(I_{CO})} = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}}$ or $S_{(I_{CO})} = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}}$ ... (1)

ii) $S_{(V_{BE})} = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$ or $S_{(V_{BE})} = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$ ... (2)

iii) $S_{(\beta)} = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}}$ or $S_{(\beta)} = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}}$ ... (3)

Key Point

1. Ideally, stability factor should be perfectly zero to k operating point stable.
2. Practically stability factor should have the value minimum as possible. Thermal stability of a circuit assessed by deriving a stability factor, S.
3. Stability factor indicates the degree of change in operat point due to variation in temperature.

Q.65 Derive the expression for the stability factor S of the fi bias circuit.

Ans. : Step 1 : Obtain the value of $\partial I_B / \partial I_C$

For fixed bias circuit,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$\frac{\partial I_B}{\partial I_C} = 0$$

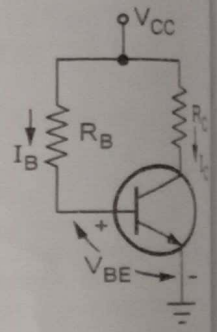


Fig. Q.65.1

Step 2 : Substituting the value of $\partial I_B / \partial I_C$ in expression of S.

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} + \frac{1+\beta}{1-0} = 1+\beta$$

Q.66 State the stability factor $S_{(ICO)}$ for voltage divider bias collector feedback bias circuits.

Ans. :

$$S_{(ICO)} = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

... For voltage divider

$$S_{(ICO)} = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta\ \text{constant}} = \frac{1-\beta}{1-\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

... For collector feedback bias circuit

Q.67 What is meant by compensation techniques ?

Ans. : Compensation techniques refer to the use of temperature-sensitive devices such as diodes, transistors, thermistors, etc., which provide compensating voltages and currents to maintain the operating point stable.

Q.68 Explain the diode compensation technique used in voltage divider bias circuit.

Ans. : Fig. Q.68.1 shows diode compensation technique used in voltage divider bias.

Here, diode is connected in series with resistance R_2 in the voltage divider circuit and it is forward biased condition.

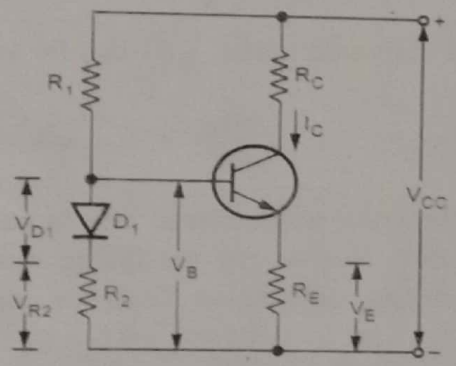


Fig. Q.68.1 Diode compensation in voltage divider bias circuit

We derived for voltage divider bias,

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Also,

$$I_E = \frac{V_E}{R_E}$$

and

$$I_C \approx I_E$$

$$\therefore \quad I_C \approx \frac{V_B - V_{BE}}{R_E} \quad \ldots (1)$$

When V_{BE} changes with temperature, I_C also changes.

To cancel the change in I_C, one diode is used in this circuit for compensation as shown in Fig. Q.68.1. The voltage at the base V_B is now,

$$V_B = V_{R2} + V_D$$

Substituting in equation (1), we get,

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E} \quad \ldots (2)$$

If the diode which is used in this circuit is of same material and type as the transistor, the voltage across the diode will have the same temperature coefficient ($-2.5\ mV/°C$) as the base to emitter voltage V_{BE}. So when V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D and $\partial V_D \approx \partial V_{BE}$, the changes tend to cancel each other and leave the collector current as

$$I_C \approx \frac{V_{R2}}{R_E}$$

Which is unaffected due to change in V_{BE}. From Fig. Q.68.1 we can see that biasing is provided by R_1, R_2 and R_E. The changes in V_{BE} due to temperature are compensated by changes in the diode voltage which keeps I_C stable at Q point.

Q.69 What is thermal runaway ?

Ans. : The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increase in the collector current. The process is cumulative and it is referred to as **self heating**. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called '**Thermal runaway**' of the transistor.

Q.70 Derive the equation to avoid thermal runaway.

Ans. : The required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated. It is given by,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \ldots (1)$$

If we differentiate equation

$T_j - T_A = \theta P_D$ with respect to T_j we get,

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\therefore \frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \quad \ldots (2)$$

Now substituting equation (2) in equation (1) we get

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \quad \ldots (3)$$

This condition must be satisfied to prevent thermal runaway. By proper design of biasing circuit it is possible to ensure that the transistor cannot runaway below a specified ambient temperature or even under any condition.

Let us consider voltage divider bias circuit for the analysis.

From the Fig. Q.70.1 we can say that,

P_C = Heat generated at the collector junction

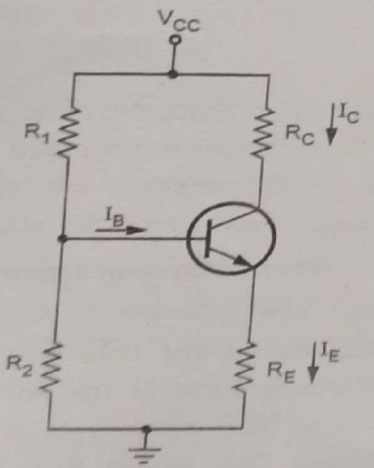


Fig. Q.70.1 Voltage divider bias circuit

= D.C. Power input to the circuit – the power lost as I^2R in R_C and R_E

$$\therefore P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E \quad \ldots (4)$$

If we consider $I_C \cong I_E$ we get

$$P_C = V_{CC} \times I_C - I_C^2 (R_C + R_E) \quad \ldots (5)$$

Differentiating equation (5) with respect to I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2 I_C (R_C + R_E) \quad \ldots (6)$$

Referring and rewriting condition equation (3) to avoid thermal runaway we get,

$$\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \quad \ldots (7)$$

In the above equation $\frac{\partial I_D}{\partial T_j}$ can be written as,

$$\frac{\partial I_D}{\partial T_j} = S \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j} \quad \ldots (8)$$

Since junction temperature affects collector current by affecting I_{CO} V_{BE}, and β. But as we are doing analysis for thermal runaway the affect of I_{CO} dominates. Thus we can write

$$\frac{\partial I_C}{\partial T_j} = \frac{\partial I_{CO}}{\partial T_j} \quad \ldots (9)$$

As the reverse saturation current for both silicon and germanium increases about 7 percent per °C, we can write

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07 I_{CO} \quad \ldots (10)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ in equation (9) we get

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07 I_{CO} \quad \ldots (11)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ from equations (11) and (6) into equation (7) we get,

$$[V_{CC} - 2 I_C (R_C + R_E)] (S) (0.07 I_{CO}) < \frac{1}{\theta} \quad \ldots (12)$$

As S, I_{CO} and θ are positive, we see that the inequality in equation (14) is always satisfied provided that the quantity in the square bracket is negative.

$$\therefore \quad V_{CC} < 2 I_C (R_C + R_E)$$

$$\therefore \quad \frac{V_{CC}}{2} < I_C (R_C + R_E) \quad \ldots (13)$$

Applying KVL to the collector circuit of Fig. Q.70.1 we get,

$$V_{CE} = V_{CC} - I_C (R_E + R_C) \quad \because \quad I_C \cong I_E$$

$$\therefore \quad I_C (R_E + R_C) = V_{CC} - V_{CE}$$

Substituting value of $I_C (R_E + R_C)$ in equation (13) we get,

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$\therefore \quad V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$\therefore \quad V_{CE} < \frac{V_{CC}}{2}$$

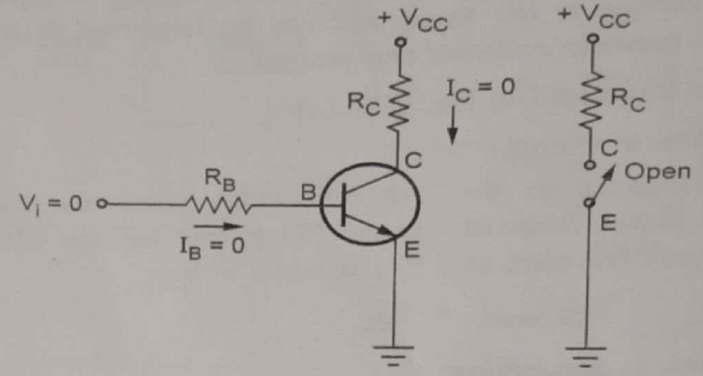
Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured. But in transformer coupled circuit, R_C and R_E are quite small and $V_{CE} \cong V_{CC}$. Hence it is necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway.

2.11 : Biasing BJT Switching Circuits

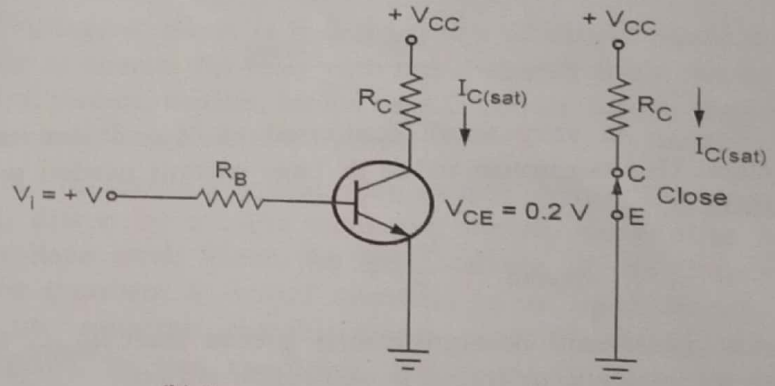
Q.71 Explain the operation of BJT as a switch.

OR Draw and explain the direct coupled switching circuit.

Ans. : • Second major application area of BJT is switching applications. When used as an electronic switch, a BJT is normally operated alternately in cut - off and saturation.



(a) Operated in cut-off (open switch)



(b) Operated in saturation (closed switch)

Fig. Q.71.1

• When $V_i = 0$, emitter - base junction is reverse biased and transistor is in cut - off region. In this condition, $I_B = I_C = 0$ and there is open circuit between collector and emitter. This is illustrated in Fig. Q.71.1 (a).

- When V_i = + V, emitter - base junction is forward biased. In this condition, base current flows and it is greater than I_C/β, hence transistor is operated in saturation region. In saturation condition, voltage between collector and emitter, $V_{CE(sat)}$ is typically 0.2 V. This voltage is too small and can be neglected to treat a short circuit between collector and emitter.
- This is illustrated in Fig. Q.71.1 (b).

Conditions in Cutoff :

A transistor is in the cut - off region when the base - emitter junction is not forward - biased. Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC}.

$$V_{CE(cutoff)} = V_{CC}$$

Conditions in Saturation :

When the base - emitter junction is forward - biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is,

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

Since $V_{CE(sat)}$ is very small compared to V_{CC}, it can usually be neglected. The minimum value of base current needed to produce saturation is,

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

Normally, I_B should be significantly greater than $I_{B(min)}$ to ensure that the transistor is operated in saturation region.

Q.72 For the circuit shown in Fig. Q.72.1.
i) Determine the value of V_{CE} when V_{IN} = 0 V.
ii) Calculate minimum value of I_B to saturate transistor if β_{dc} is 100 ? Assume $V_{CE(sat)}$ = 0.2 V.
iii) Calculate the maximum value of R_B when V_{IN} = 5 V.

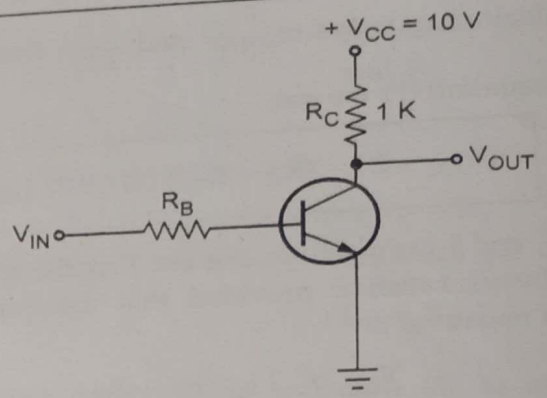


Fig. Q.72.1

Ans. : i) When V_{IN} = 0, transistor is in cut-off and

$$V_{CE} = V_{CC} = \mathbf{10\ V}$$

ii) $$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.2}{1K} = \mathbf{9.8\ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{9.8\,mA}{100} = \mathbf{98\ \mu A}$$

This is minimum value of I_B to drive the transistor to the point saturation.

Any further increase in I_B will ensure the transistor operation saturation region.

iii) When V_{IN} = 5 V, transistor in ON and

V_{BE} = 0.7 V.

∴ Voltage across R_B

$$(V_{RB}) = V_{IN} - 0.7 = 5 - 0.7 = \mathbf{4.3\ V}$$

The maximum value of R_B

$$(R_{B(max)}) = \frac{V_{RB}}{I_{B(min)}} = \frac{4.3\,V}{98\,\mu A} = \mathbf{43.88\ k\Omega}$$

Q.73 Explai

Ans. : Fig. turn off an input voltag off-time) is

V_{in} 0

- When the reverse bia collector cu light.
- When the junction is operate the I_B flows ar current thro on for 0.5 s

Q.74 Draw ar BJT to turn O

Ans. : • Rela electromagnet position to a c

Q.73 Explain the transistor circuit to switch ON/OFF an LED.

Ans. : Fig. Q.73.1 shows how transistor can be used as a switch to turn off and turn on LED. As shown in Fig. Q.73.1, square wave input voltage with a period of 1 sec (0.5 sec on-time and 0.5 sec off-time) is applied to the input.

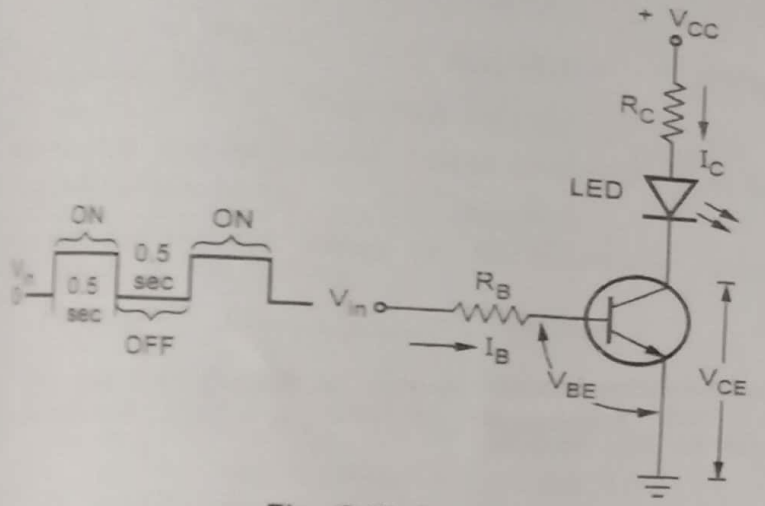


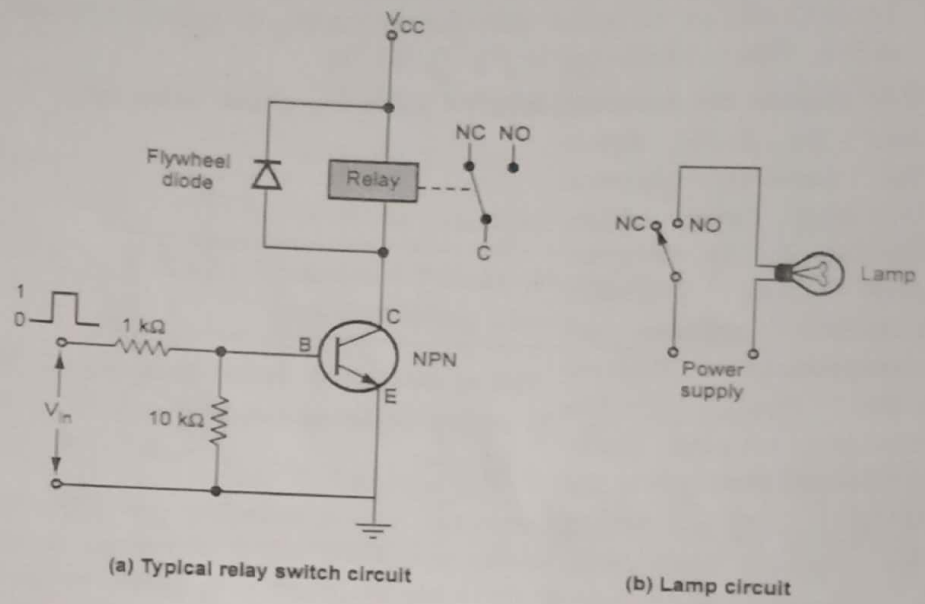
Fig. Q.73.1

When the square wave is at 0 V, the base emitter junction is reverse biased and the transistor is in cut-off. As a result, collector current I_c is zero and hence the LED does not emit light.

When the square wave goes to its high level, the base emitter junction is forward biased and there is enough base current to operate the transistor in saturation. As a result, collector current flows and it forward-biases the LED. The resulting collector current through the LED causes it to emit light. Thus, the LED is on for 0.5 second and off for 0.5 second.

Q.74 Draw and explain the working of relay switch circuit using BJT to turn OFF/ON lamp.

Ans. : • Relays are electromechanical devices that use an electromagnet to operate a pair of movable contacts from an open position to a closed position.



(a) Typical relay switch circuit (b) Lamp circuit

Fig. Q.74.1

- The advantage of relays is that it takes a relatively small amount of power to operate the relay coil, but the relay itself can be used to control motors, heaters, lamps or AC circuits which themselves can draw a lot more electrical power.
- Fig. Q.74.1 (a) shows a typical relay switch circuit. The circuit has the coil driven by a NPN transistor switch, depending on the input voltage level. When the base voltage of the transistor is zero, the transistor is cut-off and acts as an open switch. As a result no collector current flows and the relay coil is de-energized. In this condition, NC (normally closed) contact remains close and normally open contact remains open.
- When the base voltage of the transistor is sufficient enough to drive the transistor in saturation, transistor acts as a close switch. As a result, collector current flows and the relay coil is energized. In this condition, NC (normally closed) contact gets open and normally open contact gets close.

• We can connect lamp, heater or any other device connecting NO/NC contact in series with power supply to control ON/OFF action. This is illustrated in Fig. Q.74.1 (b).

Q.75 Explain the capacitor coupled Switching circuit using BJT.

Ans. : Fig. Q.75.1 shows the capacitor coupled switching circuit. Here, resistor R_B is designed such that normally transistor operates in saturation, i.e. in ON-State with $V_{CE(Sat)}$. The capacitor coupled (pulse waveform) input turns the device off giving $V_{CE} = V_{CC}$

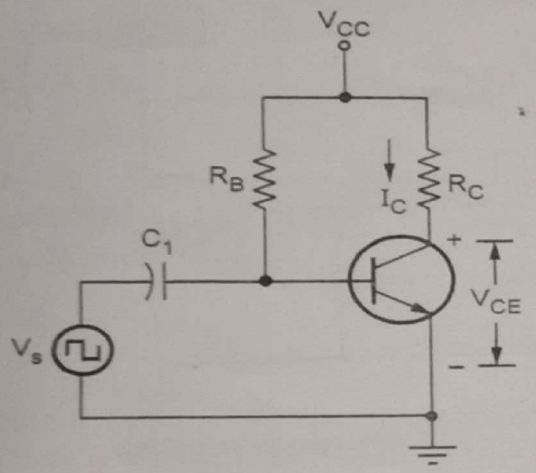


Fig. Q.75.1 Capacitor coupled switching circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CE(sat)} = V_{CC} - I_C R_C$$

Neglecting $V_{CE(sat)}$ we have

$$I_C R_C \approx V_{CC}$$

The minimum current gain is given by

$$h_{FE(min)} = \frac{I_C}{I_B}$$

Q.76 Calculate the minimum h_{FE} required for transistor to operate as a switch shown in Fig. Q.76.1. (See Fig. Q.76.1 on next page)

Ans. :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{15 - 0.7}{56K}$$

$$= 255\ \mu A$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$= \frac{15 - 0.2}{3.3\ K}$$

$$= 4.48\ mA$$

$$h_{FE(min)} = \frac{I_C}{I_B}$$

$$= \frac{4.48\,mA}{255\ \mu A}$$

$$= 17.57$$

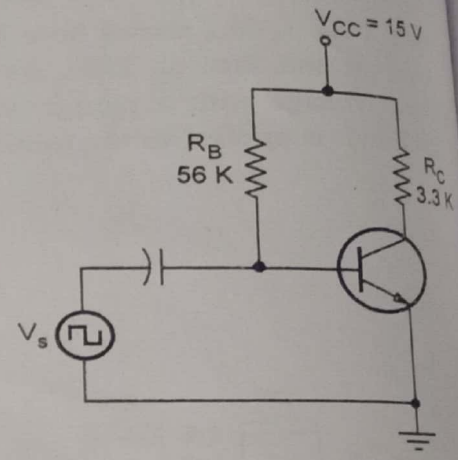


Fig. Q.76.1

Q.77 For switching circuit shown in Fig. Q.77.1 has V_{CC} = 12 V, I_C = 1.5 mA. $h_{FE(min)}$ = 10 and V_S = +5 V. Determine suitable resistances for R_B and R_C

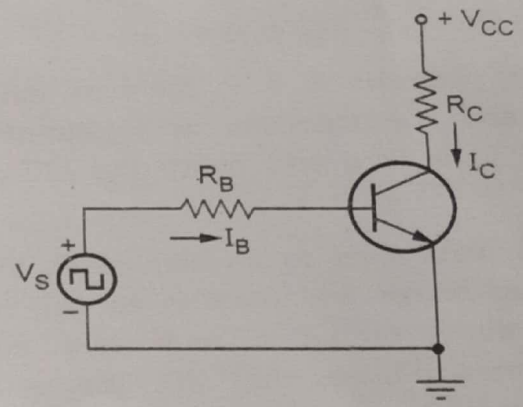


Fig. Q.77.1

Ans. :

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C} = \frac{12 - 0.2}{1.5\ mA}$$

$$= 7.87\ k\Omega$$

$$\approx 8.2\ k\Omega \text{ (Standard value)}$$

$$I_B = \frac{I_C}{h_{FE(min)}} = \frac{1.5\,mA}{10}$$

$$= 150\ \mu A$$

$$R_B = \frac{V_S - V_{BE}}{I_B} = \frac{5 - 0.7}{150\,\mu A}$$

$$= 28.6\ k\Omega$$

$$= 27\ k\Omega \text{ (Standard value)}$$

... use nearest standard lower value to ensure that I_B is ... required for saturation.

... suitable resistor values for the capacitor coupled ... circuit shown in Fig. Q.78.1.

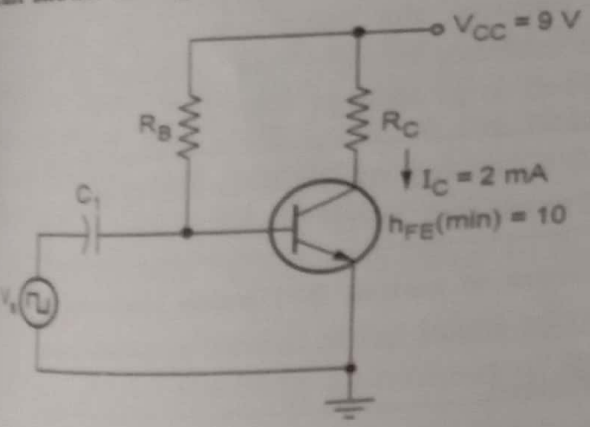


Fig. Q.78.1

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C} = \frac{9 - 0.2}{2\ mA}$$

$$= 4.4\ k\Omega$$

$$= 4.7\ k\Omega \text{ (Standard value)}$$

$$I_B = \frac{I_C}{h_{FE(min)}}$$

$$= \frac{2\,mA}{10} = 200\ \mu A$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{9V - 0.7}{200\,\mu A}$$

$$= 41.5\ k\Omega$$

$$= 39\ k\Omega \text{ (Standard value)}$$

2.12 : Transistor Power Dissipation and Switching Times

Q.79 Comment on power dissipation in BJT.

Ans. : The quiescent power dissipation in BJT is

$$P_{DQ} = V_{CEQ} I_C$$

It says that the quiescent power dissipation equals the dc voltage times dc current. It is the worst case power dissipation. Therefore, the power rating of a transistor amplifier circuits must be greater than P_{DQ}

Q.80 Explain with relevant diagram the various transistor switching times.

Ans. : Let us see Fig. Q.80.1. When the base input current is applied, the transistor does not switch on immediately. This is because of the junction capacitance and the transition time of electrons across the junctions. The time between the application of the input pulse and the commencement of collector current flow is termed as **delay time** t_d, and the time required for I_C to reach 90 % of its maximum level from 10 % level is called the **rise time** t_r. Thus the turn-on time t_{ON} is the addition of t_r and t_d ($t_{ON} = t_d + t_r$).

Similarly, when input current I_B is switched OFF, I_C does not go to zero level immediately. It goes to zero level after turn off time, which is the sum of **storage time** t_s and **fall time** t_f as shown in the Fig. Q.80.1. The fall time is specified as the time required for I_C to go from 90 % to 10 % of its maximum level.

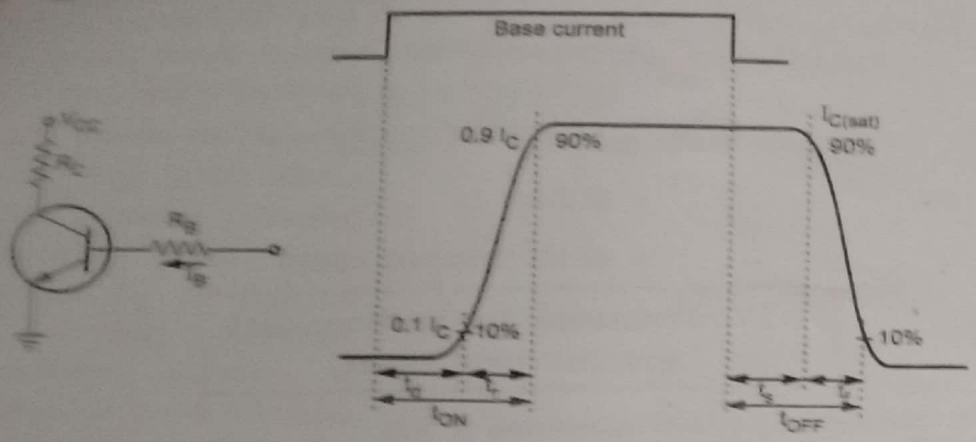


Fig. Q.80.1 Transistor turn-ON and turn-OFF times

Delay Time

It is the time that elapses between the application of the input pulse and current to rise to 10 percent of it maximum (saturation) value $I_{C\,sat} \approx V_{CC}/R_C$. The delay time exists due to following reasons.

- When the driving signal is applied to the transistor input, a non-zero time is required to charge up the emitter junction transition capacitance so that the transistor may be brought from cut-off to the active region.
- Even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a time interval is required before these carriers can cross the base region to the collector junction and be recorded as collector current.
- Finally, some time is required for the collector current to rise to 10 percent of its maximum.

Rise Time and Fall Time

The time required for I_C to reach 90% of its maximum level from 10% level is called the **rise time** (t_r), and time required for I_C to go from 90% to 10% of its maximum level is called **fall time** (t_f). The

rise time and the fall time are due to the fact that, if a base current step is used to saturate the transistor or return if from saturation to cutoff, the transistor collector current must traverse the active region. The collector current increases or decreases along an exponential curve whose time constant is τ_r. It is given by,

$$\tau_r = h_{FE}(C_C R_C + 1/\omega_T)$$

where C_C is the collector transition capacitance and ω_T is the radian frequency at which the current gain is unity.

Storage Time

When transistor is in saturation, it has excess minority carriers stored in the base. The transistor cannot respond until this saturation excess charge has been removed. Due to this there is a finite time elapses between the transition of the input waveform and the time when collector current has dropped to 90 percent of $I_{C(sat)}$ and it is referred to as **storage time** (t_s).

2.13 : Testing of Bipolar Junction Transistor with Multi-Meter

Q.81 Explain the process of testing BJT using multi-meter.

Ans. : Transistor can be tested using following procedure :

Step 1 : (Base to Emitter)

Hook the positive lead from the multi-meter to the BASE (B) of the transistor. Hook the negative meter lead to the EMITTER (E) of the transistor. For good NPN transistor, the meter should show a voltage drop between 0.45 V and 0.9 V. If you are testing PNP transistor, you should see "OL" (Over Limit).

Step 2 : (Base to Collector)

Keep the positive lead on the BASE (B) and place the negative lead to the COLLECTOR (C). For good NPN transistor, the meter should show a voltage drop between 0.45 V and 0.9 V. If you are testing PNP transistor, you should see "OL" (Over Limit).

Step 3 : (Emitter to Base)

Hook the positive lead from the multi-meter to the EMITTER (E) of the transistor. Hook the negative meter lead to the BASE (B) of the transistor. For good NPN transistor, you should see "OL" (Over Limit). If you are testing PNP transistor, the meter should show a voltage drop between 0.45 V and 0.9 V.

Step 4 : (Collector to Base)

Hook the positive lead from the multi-meter to the COLLECTOR (C) of the transistor. Hook the negative meter lead to the BASE (B) of the transistor. For good NPN transistor, you should see "OL" (Over Limit). If you are testing PNP transistor, the meter should show a voltage drop between 0.45 V and 0.9 V.

Step 5 : (Collector to Emitter)

Hook the positive meter lead to the COLLECTOR (C) and the negative meter lead to the EMITTER (E) - A good NPN or PNP transistor will read "OL"/Over Limit on the meter. Swap the leads (Positive to Emitter and Negative to Collector) - Once again, a good NPN or PNP transistor should read "OL".

If your bipolar transistor measures contrary to these steps, consider it to be bad.

2.14 : Reading Datasheet of BJT

Q.82 List the important rating of BJT specified in the datasheet.

Ans. : 1. V_{CEO} : It is a d.c. collector-emitter breakdown voltage with base open-circuited.

2. V_{CB} : It is a d.c. collector-base breakdown voltage for reverse biased collector-base junction.

3. V_{EB} : It is a d.c. emitter-base breakdown voltage for reverse biased emitter-base junction.

4. $P_{D(max)}$: It specifies the maximum power dissipation allowed for the device.

5. $I_{C(min/max)}$: It specifies minimum and maximum values of collector current.

6. $h_{fe(min)}$: It specifies minimium current gain.

Along with these specifications, data sheet also provides values for output capacitance, input capacitance delay time, rise time, storage time and fall time.

END...

3 Special Purpose Diodes and Transistors

3.1 : Light Emitting Diode (LED)

Q.1 What is LED ? Draw its symbol and explain its construction.

Ans. : • A diode which emits light when forward biased is called a Light Emitting diode (LED).

- In LED three semiconductor layers on the substrate are used as shown in the Fig. Q.1.1 (a).
- In between p type and n type region, there exists a region called active region. This region is responsible for the emission of the light.
- The LED emits light all the way around the layered structure. This layered structure is placed in a tiny reflective cup so that the light gets reflected towards the desired exit direction. This cup type structure is shown in the Fig. Q.1.1 (b).
- The symbol of the LED is shown in the Fig. Q.1.1 (c).

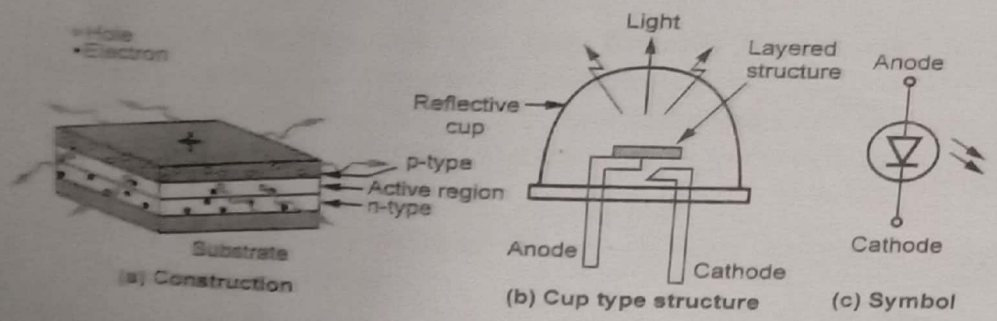
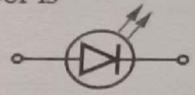


Fig. Q.1.1 LED

Q.2 Compare LED with P-N junction diode.

Ans. :

Sr. No.	LED	P-N junction diode
1.	It emits light, when forward biased.	It does not emit light.
2.	It uses materials like gallium, arsenide phosphide and gallium phosphide.	It uses materials like silicon and germanium.
3.	The drop across forward biased LED is about 2 V.	The drop across forward biased diode is about 0.7 V, much less than that of LED.
4.	Reverse breakdown voltage is low, about 3 V to 10 V.	Reverse breakdown voltage is high, about 50 V and more.
5.	Needs large power for the operation.	Needs less power for the operation.
6.	Draws considerable current from battery.	Draws less current.
7.	Symbol is 	Symbol is 
8.	The applications are optocouplers, seven segment displays, alpha numeric displays.	The applications are rectifiers, clippers, clampers, voltage multipliers and many other electronic circuits.

Q.3 State the advantages, disadvantages and applications of LED.

Ans. : • The various **advantages** of LED are,

1. Small in size.
2. Very fast in operation.
3. Have long lilfe.
4. Cheap and readily available.

5. Easy to interface with various other electronic circuits.
6. Light in weight.
7. Available in various colours.

The various **disadvantages** of LED are,

1. Draws considerable current requiring frequent replacement of battery in low power battery operated devices.
2. Low luminous efficiency.
3. Temperature dependent characteristics.
4. Need large power for the operation than normal diode.

The various **applications** of LED are,

1. All kinds of visual displays i.e. seven segment displays and alpha numeric displays. Such displays are commonly used in the watches and calculators.
2. In the optical devices such as optocouplers.
3. As on-off indicator in various types of electronic circuits.
4. Some LEDs radiate infrared light which is invisible. But such LEDs are useful in remote controls and applications like burglar alarm.

Q.4 Explain the working principle of LED.

Ans. : • The LED works on the principle of **electroluminescence**.

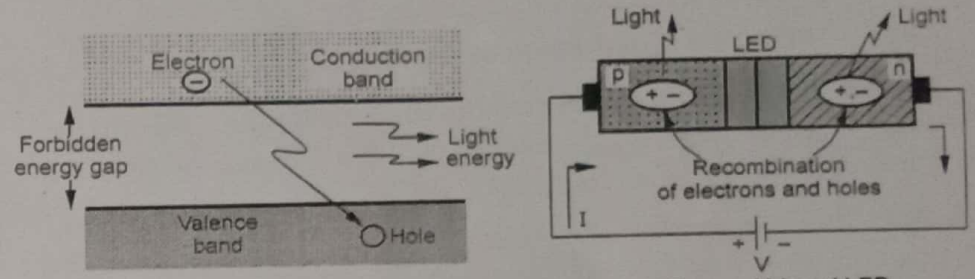
When a p-n junction is forward biased, the electrons in n region cross the junction and recombine with holes in p region.

The free electrons exist in the conduction band while the holes exist in the valence band.

The energy level of free electrons is higher than the energy level of the holes.

When electrons recombine with the holes, they move from conduction band to valence band which is at lower energy level.

- While moving, the difference between the energy levels of conduction band and valence band is released by the free electrons which appears in the form of light due to the special material used in the LED.
- The Fig. Q.4.1 shows the principle of working of LED.



(a) Process of electroluminescence (b) Forward biased LED

Fig. Q.4.1 Principle of operation of LED

- The energy released depends on the forbidden gap energy which determines the wavelength and the colour of the emitted light.

3.2 : Zener Diode

The zener diode is already discussed in the Section 1.10.

3.3 : Zener Diode Circuit for Voltage Regulation

Important Points to Remember

- A circuit used after the filter circuit in a power supply which makes the d.c. output voltage smooth and ripple free and keeps it constant irrespective of changes in the load or in input line voltage is called voltage regulator.

Q.5 Explain the use of zener diode for voltage regulation under varying line voltage and load.

Ans. : • A shunt voltage regulator using zener diode is shown in the Fig. Q.5.1.

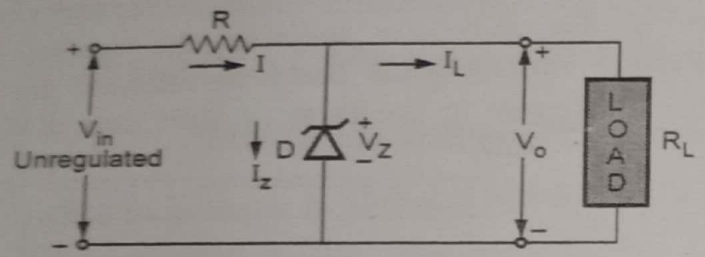


Fig. Q.5.1 Zener diode as a shunt regulator

- The zener diode has a characteristics that as long as the current through it is between I_{Zmin} and I_{Zmax}, the voltage across it is constant equal to zener voltage V_Z.
- As zener diode is connected in shunt with the load resistance, the output voltage is equal to the zener voltage.
- From the Fig. Q.5.1 we can write,

$$V_o = V_Z \quad \text{and} \quad I = I_Z + I_L$$

Regulation with varying input voltage :

- The load current $I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L}$ = constant and $I = I_Z + I_L$.
- If V_{in} increases, then the total current I increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant.
- Similarly if V_{in} decreases, then current I decreases. But to keep I_L constant, I_Z decreass.
- But in both cases, as long as I_Z is between I_{Zmin} and I_{Zmax}, the V_Z i.e. output voltage V_o is constant.
- **Thus the changes in input voltage get compensated and output is maintained constant.**

Regulation with varying load :

- The input voltage is constant while the load resistance R_L is variable.

- As V_{in} is constant and $V_o = V_Z$ is constant, then for constant R the current I is constant.

$$\therefore \quad I = \frac{V_{in} - V_Z}{R} \text{ constant } = I_L + I_Z$$

- If R_L decreases, I_L increases and to keep I constant I_Z decreases accordingly. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant.
- Similarly if R_L increases, I_L decreases and to keep I constant I_Z increases accordingly. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant.
- **Thus the changes in the load get compensated and output is maintained constant.**

Q.6 For a zener regulator shown in the Fig. Q.6.1, calculate the range of input voltage for which output will remain constant.
V_Z = 6.1 V, I_{Zmin} = 2.5 mA, I_{Zmax} = 25 mA, r_Z = 0 Ω

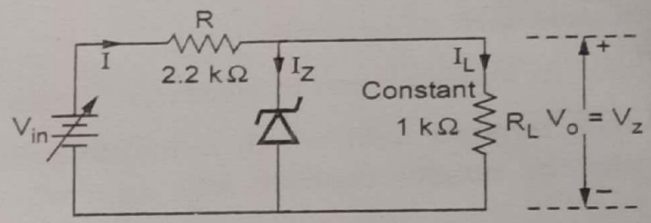


Fig. Q.6.1

Ans. : R_L = 1 kΩ, V_Z = 6.1 V

$$\therefore \quad I_L = \frac{V_Z}{R_L} = \frac{6.1}{1\times10^3} = 6.1 \text{ mA constant}$$

For $V_{in(min)}$, $I_Z = I_{Zmin}$ = 2.5 mA

$$\therefore \quad I = I_{Zmin} + I_L = 2.5 + 6.1 = 8.6 \text{ mA}$$

$$\therefore \quad V_{in(min)} = V_Z + IR$$

$$= 6.1 + 8.6\times10^{-3}\times2.2\times10^3$$

$$= 25.02 \text{ V}$$

For $V_{in(max)}$

$$I_Z = I_{Zmax} = 25 \text{ mA}$$

$$I = I_{Zmax} + I_L = 25 + 6.1 = 31.1 \text{ mA}$$

$$V_{in(max)} = V_Z + IR$$

$$= 6.1 + 31.1\times10^{-3} \times 2.2\times10^{3}$$

$$= 74.52 \text{ V}$$

Thus the range of input voltage is **25.02 V** to **74.52 V**, for which output will be constant.

Q.7 A zener diode has a breakdown voltage of 10 V. It is supplied from a voltage source varying between 20 - 40 V in series with a resistance of 820 Ω. Using an ideal zener model obtain the minimum and maximum zener currents.

Ans. : The circuit is shown in the Fig. Q.7.1.

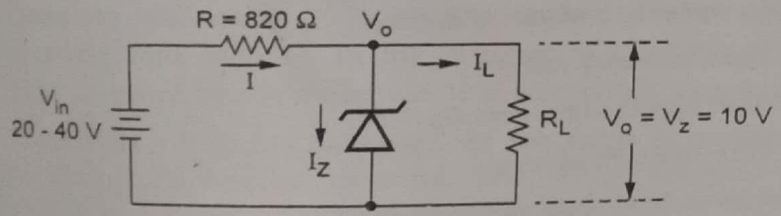


Fig. Q.7.1

$$I = \frac{V_{in} - V_o}{R}$$

$$I = \frac{V_{in} - 10}{820}$$

$$I_{max} = \frac{V_{in(max)} - 10}{820}$$

$$= \frac{40 - 10}{820} = 36.585 \text{ mA}$$

$I_{Z\,min} = 0$ A ...For ideal Zener diode

Now $I = I_Z + I_L$

$\therefore$ $I_{max} = I_{Zmin} + I_{L(max)}$

$\therefore$ $I_{L(max)} = I_{max} = 36.585$ mA

when $I_L = I_{L(min)}$

$= 0$ A ... Open load terminals

under this condition if $V_{in} = V_{in(max)}$ then,

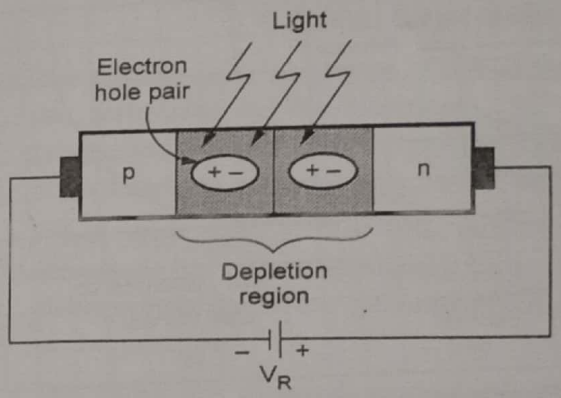
$I = 36.585$ mA

and $I_Z = I_{Zmax} = 36.585$ mA

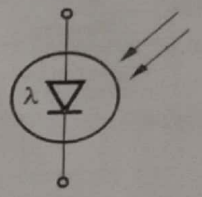
3.4 : Photodiode

Q.8 Explain the working of photodiode along with its characteristics. Why photodiode is operated in reverse biased condition when operated as a optical detector ?

Ans. : • The Fig. Q.8.1(a) shows the construction of a photodiode and the Fig. Q.8.1(b) shows the symbol of a photodiode.



(a) Construction



(b) Symbol

Fig. Q.8.1 Photodiode

- The glass lens is fixed over the junction through which the light is incident on the junction.
- Due to reverse biasing, the depletion region is wide.

- When the photons of light strike the depletion region, they give energy to the ions and generate the electron-hole pairs.
- The number of electron-hole pairs depend on the intensity of the light.
- Due to increased minority carriers, the reverse current increases, which is nothing but a photocurrent.
- More the light intensity, more is the number of electron-hole pairs and more is the photocurrent.
- The reverse current is directly proportional to the intensity of the light and is not dependent on the reverse voltage.
- The graph of V_R and reverse current I_λ for various light intensities is called **characteristics of photodiode**.
- The Fig. Q.8.2 (a) shows the graph of reverse current and V_R for various intensities while the Fig. Q.8.2 (b) shows the graph of reverse current against light intensity.

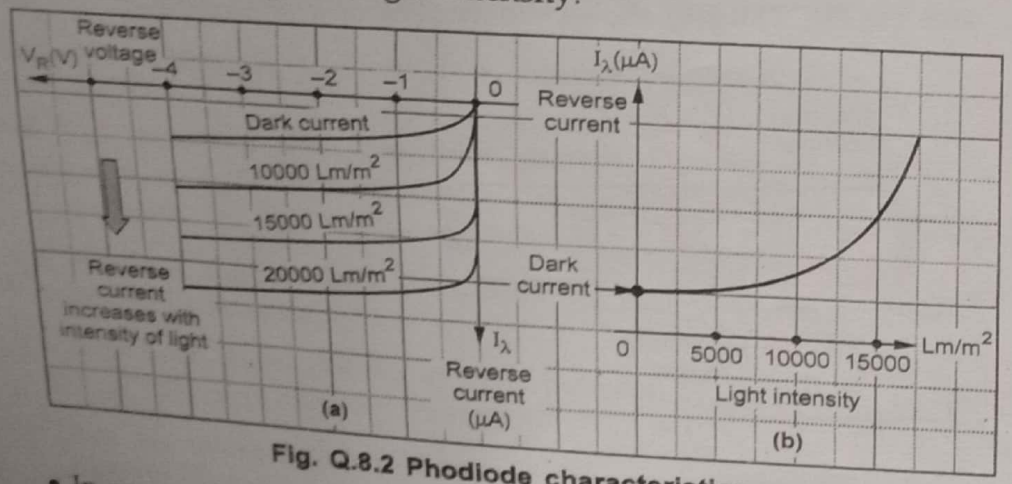


Fig. Q.8.2 Phodiode characteristics

- In reverse biased, the minority charge carriers control the current which are less in number. Thus the effect of light generated carriers is significant on the reverse current.
- In forward biased, there are large number of charge carriers thus the number of light generated charge carriers is comparatively

less. Thus the applied voltage takes control of the current rather than the light. The effect of light is negligible in forward biased condition.

- Hence the **photodiode is always used in reverse biased** when used as an optical detector.

Q.9 State the applications of photodiode.

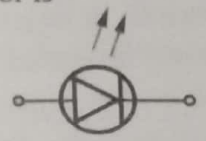
Ans. : • The various applications of photodiode are,

1. Operation is very fast hence used as a photodetector for both visible and invisible light.
2. In alarm systems.
3. For counting the objects on conveyor belt.
4. As a cell.
5. As a variable resistance device.
6. In light intensity meters.
7. In high speed logic circuits.
8. In fibre optic receivers.

Q.10 Compare LED with photodiode.

Ans. :

Sr. No.	LED	Photodiode
1.	It is a photoemitter device.	It is a photodetector device.
2.	It converts electrical energy to light energy.	It converts light energy into electrical energy in the form of current.
3.	It is operated in forward biased condition.	It is operated in reverse biased condition.
4.	More the forward current, more is the light output.	More the light intensity, more is the photocurrent.
5.	Materials used for the manufacturing are GaAs, GaAsP, GaP etc.	Materials used for the manufacturing are Si, Ge, IGaAs etc.

6.	Operating LED is cleraly visible.	Operating photodiode is not visible. It operates behind the scenes.
7.	The symbol is 	The symbol is 

Q.11 Explain the following for the a photodiode : i) Responsivity ii) Quantum efficiency iii) Directivity iv) Dark current.

Ans. : i) Responsivity : It is defined as the ratio of electrical output to the radiant light energy input. It is measured in A/W or V/W. It is a function of the wavelength of incident radiant light and also the bandgap energy of the photo detector material.

ii) **Quantum efficiency :** It is the ratio of the number of photoelectrons released to the number of photons of incident light absorbed by the materials. It is also called quantum yield.

iii) **Directivity :** It is the reciprocal of the noise equivalent power of the photo detector material. The Noise Equivalent Power (NEP) is the radiant power applied to the photo detector for which it produces an output signal equal to the root mean square noise output from the photo detector i.e. the signal to noise ratio is unity. The NEP is nothing but the minimum radiation level of the photo detector which can be detected.

iv) **Dark current :** When there is no light, the reverse biased photodiode carries a current which is very small and called dark current. It is denoted as I_λ.

3.5 : Solar Cell

Important Points To Remember

The solar cell is nothing but photovoltaic cell which works on the principle of photovoltaic effect, according to which it ... voltage proportional to the light incident on it.

Q.12 Define solar cell. Explain the construction and working of a solar cell.

Ans. : A solid state device which converts the light energy into an electrical energy based on the photovoltaic effect is called a solar cell.

- The Fig. Q.12.1 (a) shows the construction of a solar cell while the Fig. Q.12.1 (b) shows the symbol of a solar cell.

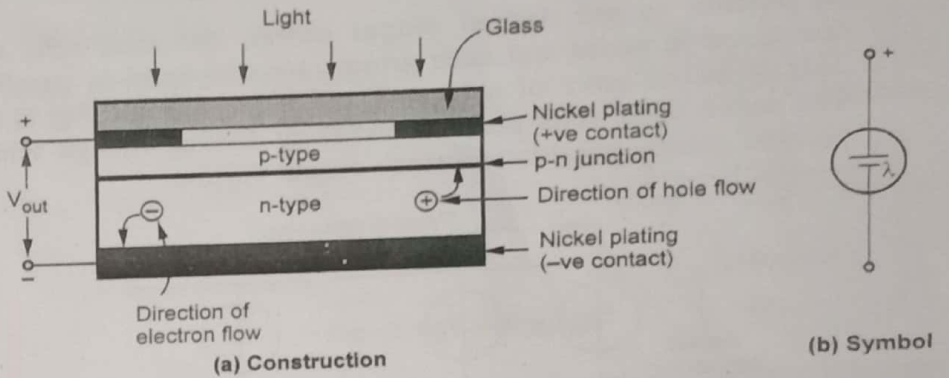


Fig. Q.12.1 Solar cell

- The surface layer of p-type material is extremely thin so that light can penetrate to the junction. The nickel plated ring around p-type is the positive output terminal. The nickel plated ring around n-type material acts as the negative output terminal.
- When the light strikes the cell, the photon light energy is absorbed by the semiconductor material and number of electron-hole pairs are generated. This happens on both the sides of the junction.
- The holes are directed towards the p-region while the electrons are directed towards the n-region due to the electric field present. Due to this movement the minority current is set up across the junction due to which the voltage is developed across the p and n regions. This voltage is taken out as the output voltage.

- The selenium and silicon are most widely used materials for the solar cells. The gallium arsenide, indium arsenide nd cadmium sulphide are also used for the solar cells.
- The efficiency of solar cell is the ratio of electrical power output to the power input by the light source. It is typically between 15 to 40 %.

Important Points To Remember

- In practice to get desired output power, the solar cells are connected in series and such groups are connected in parallel. This is called array of solar cell and shown in the Fig. Q.3.1 The series solar cells provide necessary output voltage while parallel groups provide necessary output current.

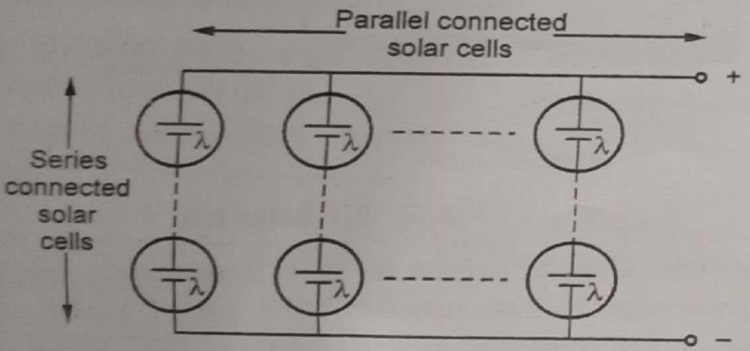


Fig. Q.3.1 Array of solar cells

Q.13 State the applications of solar cell.

Ans. : • The various applications of solar cell are,

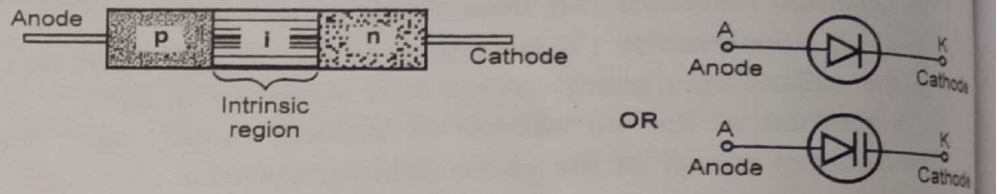
1. Satellites and space vehicles.
2. Automated street lights.
3. Power supply to calculators.
4. Emergency lights.
5. For charging the batteries.
6. Solar panels for domestic purposes, water pumps etc.

3.6 : PIN Diode

Q.14 Explain the construction and characteristics of PIN diode. Also state its applications.

Ans. : • The pin diode consists of a p and n type heavily doped materials alongwith intrinsic material. The intrinsic region is sandwitched between n type and p type.

- This is shown in the Fig. Q.14.1 (a). The symbol is shown in the Fig. Q.14.1 (b).



(a) Construction **(b) Symbol**

Fig. Q.14.1 PIN diode

- When reverse biased, its transition capacitance is predominant and constant. Hence in reversed biased condition it acts as a constant capacitance, as shown in the Fig. Q.14.1 (a).
- The characteristic of intrinsic semiconductor is such that it has low forward resistance R_F. It further decreases with increasing current. Hence pin diode acts as **current controlled variable resistance**, when forward biased. This is shown in the Fig. Q.14.2 (b).

(a) Reverse biased **(b) Forward biased**

Fig. Q.14.2 Biased PIN diode

The selenium and silicon are most widely used materials for the solar cells. The gallium arsenide, indium arsenide nd cadmium sulphide are also used for the solar cells.

The efficiency of solar cell is the ratio of electrical power output to the power input by the light source. It is typically between 15 to 40 %.

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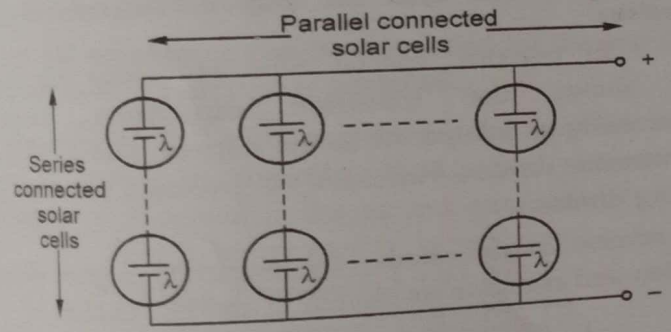

Fig. Q.3.1 Array of solar cells

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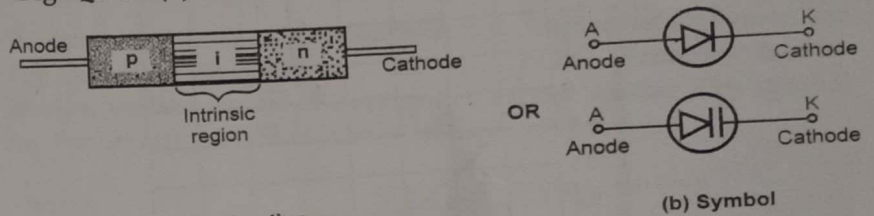

(a) Construction (b) Symbol

Fig. Q.14.1 PIN diode

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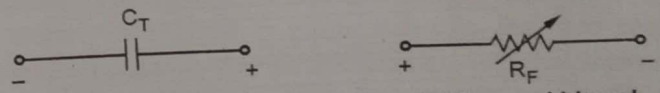


(a) Reverse biased (b) Forward biased

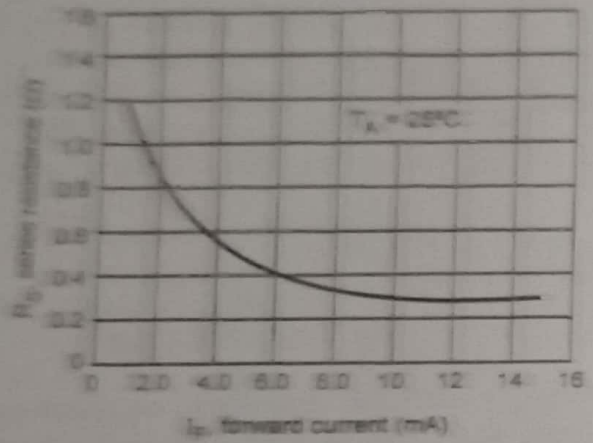
Fig. Q.14.2 Biased PIN diode

Characteristics

The pin diode has two characteristics which are,

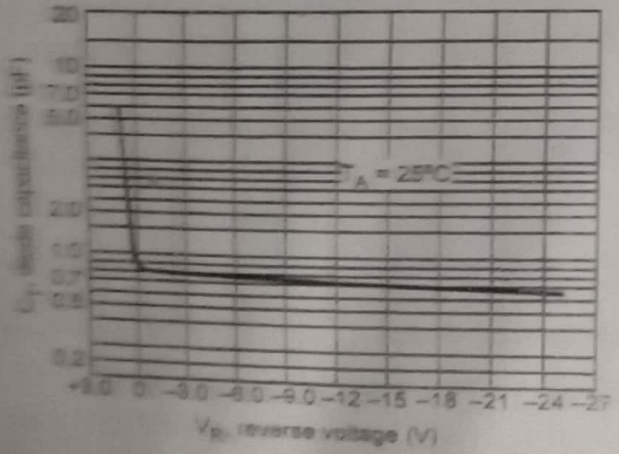
i) The forward series resistance characteristics showing the graph of forward series resistance against forward current. This is shown in the Fig. Q.14.3 (a).

ii) The reverse capacitance characteristics showing the graph of diode capacitance C_T against the reverse voltage V_R. This is shown in the Fig. Q.14.3 (b). It shows that C_T is constant.



(a)

Fig. Q.14.3 PIN diode characteristics



(b)

Fig. Q.14.3 PIN diode characteristics

Applications

- The pin diode is used in attenuator applications where resistance is required to be controlled by the current.
- The pin diode is used as a dc controlled microwave switch.
- The variable forward resistance characteristics make it suitable to be used as a modulating device.
- Some pin diodes are used as photodetectors in fibre optic systems.

3.7 : Varactor Diode

Q.15 What is varactor diode ? Explain how it can be used as variable capacitance with the help of characteristics. State its applications.

Ans. : • In practice, special type of diodes are manufactured which shows the transition capacitance property more predominantly as compared to the normal diodes. Such diodes are called **varactor diodes**, **varicap**, **VVC** (voltage variable capacitance) or **tuning diodes**.

- In a reverse baised diode, the depletion region exists between p-region and n-region as shown in the Fig. Q.15.1.

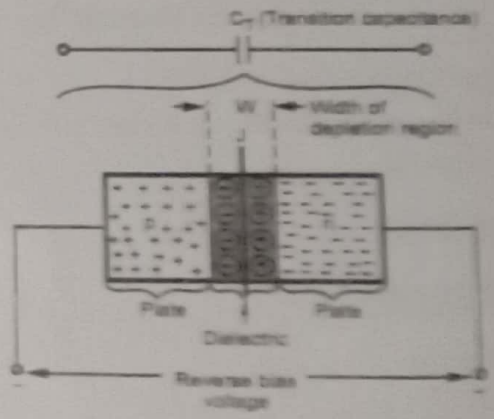


Fig. Q.15.1

- The p-region and n-region act like the plates of capacitor while the depletion region acts like dielectric.
- Thus there exists a capacitance at the p-n junction called **transition capacitance, space charge capacitance, barrier capacitance** or **depletion region capacitance**. It is denoted as C_T.
- Mathematically it is given by the expression,

$$C_T = \frac{\varepsilon A}{W}$$ where ε = Permittivity of semiconductor

A = Area of cross section and W = Width of depletion region

- As the reverse biased applied to the diode increases, the width of the depletion region (W) increases. Thus the transition capacitance C_T decreases.
- In short, the capacitance can be controlled by the applied voltage. Thus a variable capacitance is achieved.
- The variation of C_T with respect to the applied reverse bias voltage is shown in the Fig. Q.15.2. As reverse voltage is negative, graph is shown in the second quadrant.

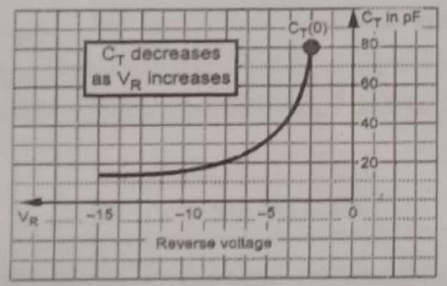


Fig. Q.15.2

- The various applications of varactor diodes are,

1. Tuned circuits
2. FM modulators
3. Automatic frequency control devices
4. Adjustable bandpass filters
5. Parametric amplifiers
6. Television receivers.

3.8 : Schottky Diode

Q.16 Explain the construction and operation of Schottky diode. Compare its characteristics with conventional diode. State its applications.

Ans. : The diodes which are specially manufactured to solve the problem of fast switching are called Schottky diodes.

- Its construction is different than the conventional p-n junction diode.
- It consists of a metal to semiconductor junction as shown in the Fig. Q.16.1(b). These diodes are also called **Schottky barrier diodes, surface barrier diodes** or **hot carrier diodes**. The symbol for the Schottky diode is shown in the Fig. Q.16.1 (a).

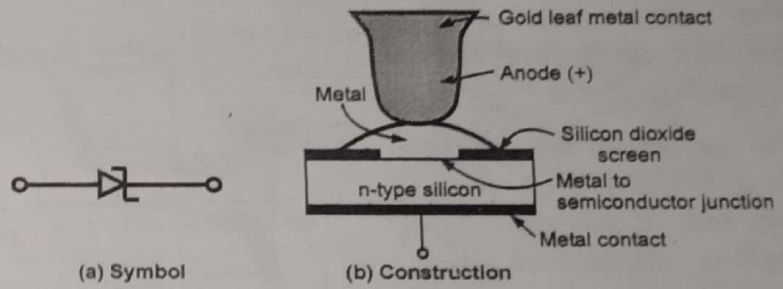


Fig. Q.16.1 Schottky diode

- In both the materials metal as well as n-type semiconductor the electrons are the majority carriers.
- In the metal, the minority carriers (holes) are very less in number. When the contact is made between the two materials, the electrons from the n-type semiconductor material immediately flow into the adjoining metal. This is because the kinetic energy level of the majority carriers i.e. electrons in the n region is higher than the electrons in the metal.
- Hence a heavy flow of majority carriers is established from n region to the metal. Due to high kinetic energy the injected carriers are called **hot carriers**.

- In conventional diode, the minority carriers get injected into adjoining region while in Schottky diode, majority carriers get injected into metal.
- In Schottky diode the conduction is totally by majority carriers.
- The heavy flow of electrons into the metal creates a region near the junction surface, depleted of carriers in the silicon material.
- The additional carriers in the metal establish a negative wall in the metal at the boundary between the two materials. This results in further current.
- So there exists a carrier free region and a negative wall at the surface of the metal.

Characteristics

- The characteristics of Schottky diode are shown in the Fig. Q.16.2.
- The barrier at the junction for a Schottky diode is less than that of normal p-n junction diode, in both forward and reverse bias region.

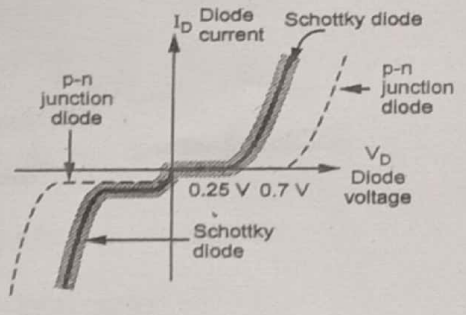


Fig. Q.16.2 Comparison of characteristics

- The barrier potential and breakdown voltage in forward bias and reverse bias region respectively are also less than p-n junction diode.
- The barrier potential of Schottky diode is 0.25 V as compared to 0.7 V for normal diode.

Applications : Due to fast switching characteristics, the Schottky diodes are very useful for high frequency applications such as digital computers, high speed TTL, radar systems, mixers, detectors in communication equipments and analog to digital converters.

3.9 : Varistor

Q.17 What is varistor ? Draw its V-I characteristics. State application.

Ans. : • In the normal power line voltage, lightning, power faults and transients cause serious problems like dips and sp The severe drop in the voltage which remains for microseconds is called dip while sudden very high voltage u 2000 V lasting for very short period of time is called spike.

- The varistor is a special device which is used for line filterin avoid the dips and spikes. It is also called a **transient suppre** due to its frequent use for protecting a.c. line from transients
- The Fig. Q.17.1 shows the symbol of varistor which is similar to two back to back connected zener diodes. In both the directions, its breakdown voltage is very high which ranges from 10 V to 1000 V. The peak transient cu capacity of varistor is hundreds or thousands of amperes.

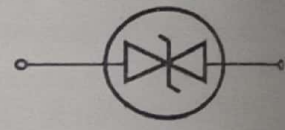


Fig. Q.17.1 Varistor sym

Characteristics

- The V-I characteristics of varistor is shown in the Fig. Q.17.2 characteristics are bilateral and similar on both sides.

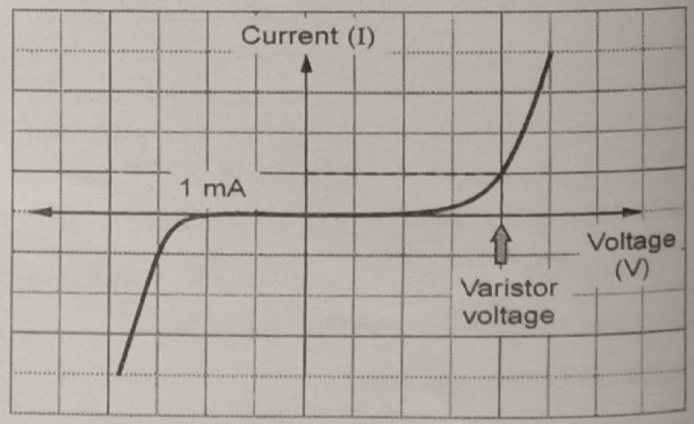


Fig. Q.17.2 V-I characteristics of varistor

- The voltage applied across the terminals when a current of 1 mA flows through varistor is called **varistor voltage.**

Applications

- The main application of varistor is the protection of circuits from transients, spikes, surges and impulse voltages. The use of varistor for protection is shown in the Fig. Q.17.3.

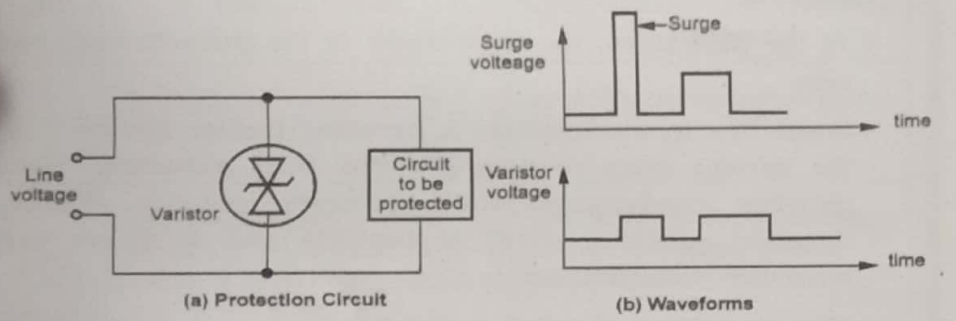


Fig. Q.17.3 Application of varistor

- When the surge voltage is below or equal to varistor voltage, the varistor works as a capacitor. But when the surge voltage exceeds the varistor voltage, the impedance across varistor terminals decreases rapidly. This directs the surge current through it bypassing the circuit to be protected. Thus surge voltage suppression is achieved.

3.10 : Tunnel Diode

Q.18 What is tunnel diode ? Explain its construction. Draw its symbol and equivalent circuit. State its applications.

Ans. : • A normal p-n junction has an impurity concentration of about 1 part in 10^8.

- The diodes in which the concentration of impurity atoms is greatly increased upto 1 part in 10^3, to get completely changed characteristics, are called Tunnel diodes.

- Due to the heavy doping, the depletion region gets reduced considerably i.e. about 1/100 the width of depletion region in normal p-n junction diode.

- Due to the thin depletion region, an electron penetrates through the barrier. This is called **tunneling** and hence such high impurity density p-n junction devices are called **tunnel diodes.** Due to such effect, it shows a **negative resistance region** in its volt-ampere characteristics.

- The most common commercially available tunnel diodes are made from the germanium or gallium arsenide.

- The basic construction of an advanced design tunnel diode is shown in the Fig. Q.18.1.

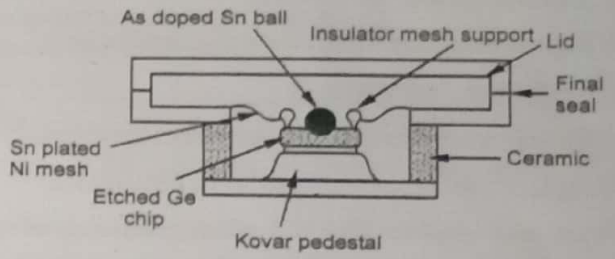


Fig. Q.18.1 Construction of tunnel diode

- The circuit symbol of a tunnel diode is shown in the Fig. Q.18.2 (a) while its equivalent circuit in the negative resistance region is shown in the Fig. Q.18.2 (b).

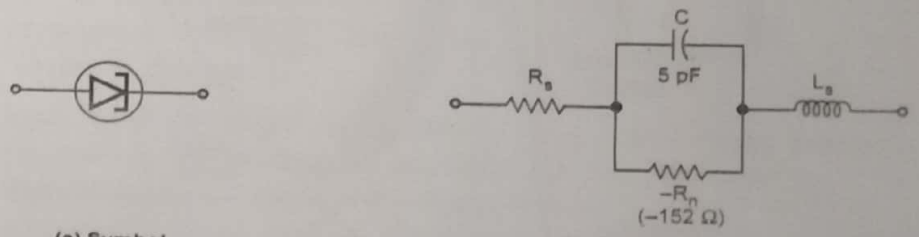


Fig. Q.18.2 Tunnel diode

- The negative resistance – R_n has a minimum value at the point of inflection between I_p and I_v.
- The series resistance R_s is due to ohmic contact resistance.
- The series inductance L_s depends upon the lead length and the geometry of the diode package.
- The junction capacitance C depends upon the bias represents the junction diffusion capacitance and is usually measured at the valley point.
- The various applications of tunnel diode are,

1. In a negative resistance oscillator.
2. As a high speed switch.
3. In pulse and digital circuits.
4. In high frequency (microwave) oscillator.
5. In switching networks
6. In timing and computer logic circuitry.
7. Design of pulse generators and amplifiers.

Q.19 Draw and explain the V-I characteristics of tunnel diode.

Ans. : • The Fig. Q.19.1 shows the volt-ampere characteristics of a tunnel diode.

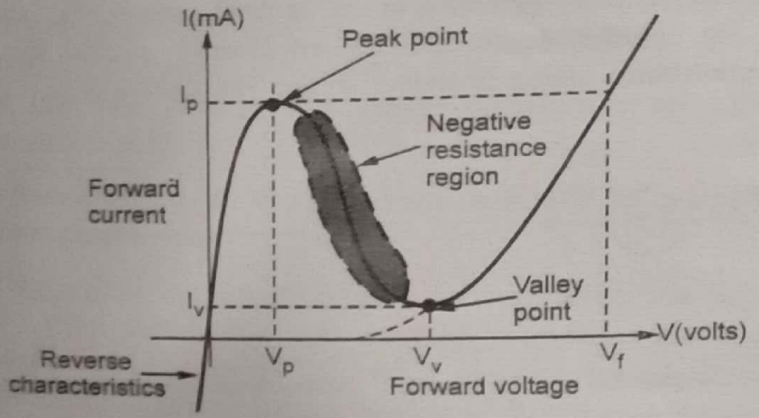


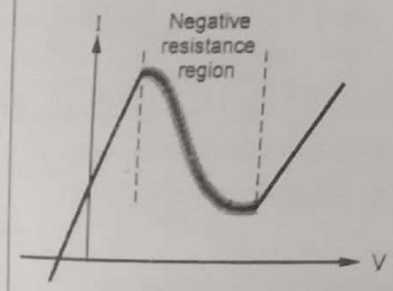
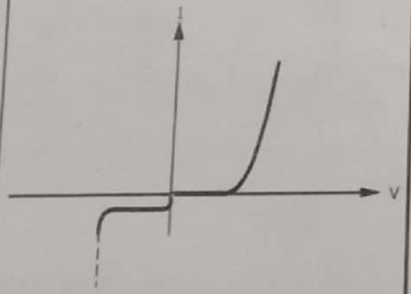
Fig. Q.19.1 Characteristics of tunnel diode

- For small forward voltages (upto 50 mV for germanium) resistance remains small, of the order of 5Ω and current increases.
- The current attains a peak value I_p corresponding to the voltage V_p which is about 600 mV.
- The I_p can vary from few micro amperes to several hundred amperes.
- At the peak point, the slope dI/dV of the characteristics becomes zero.
- If now the forward voltage is increased further, beyond V_p the current starts decreasing rather than increasing. Thus dynamic conductance dI/dV becomes negative. Hence dynamic resistance dV/dI is negative and it shows negative resistance characteristics.
- This negative resistance continues till a voltage V_v called **valley voltage**.
- At the valley voltage V_v, the current is I_v and slope becomes again zero.
- After V_v, if the voltage is increased, the current again increases. Thus resistance again becomes positive and remains positive thereafter.
- At the so called peak forward voltage V_f, the current reaches the value equal to **peak current** I_p.
- The value of current between I_p and I_v can be obtained for three different voltage values. For the value of current between I_p and I_v, the characteristics has triple values.
- This multivalued feature makes the tunnel diode useful in pulse and digital circuits.
- In the reverse direction reverse current starts at very low reverse bias voltage.

• Large reverse current flows for small reverse bias voltage hence it behaves as a good conductor in reverse direction. This is indicated in reverse characteristics.

Q.20 Compare tunnel diode with conventional p-n junction diode.

Ans. : • The comparison of tunnel diode and conventional p-n junction diode is given below.

Sr. No.	Tunnel diode	Conventional p-n junction diode
1.	Impurity concentration is high about 1 part in 10^3 atoms.	Impurity concentration is low about 1 part in 10^8 atoms.
2.	Depletion region width is about 5 microns, which is 1/ 100^{th} the width of typical p-n junction diode.	The width of depletion region is high compared to the tunnel diode.
3.	The carrier velocities are very high at low forward bias, hence can punch through the depletion region.	The carrier velocities are low at low forward bias, hence can not penetrate the depletion region.
4.	The V-I characteristics shows the negative resistance region.	The V-I characteristics does not show the negative resistance region.
5.	The V-I characteristics is, 	The V-I characteristics is, 

6.	The materials used for construction are germanium or gallium arsenide.	The silicon is most popularly used.
7.	The symbol is, 	The symbol is, 
8.	The switching time is very low of the order of nano to picoseconds.	The switching time is high.
9.	Used for high frequency oscillators, high speed applications such as computers, pulse and digital circuits and switching networks.	Used in rectifiers and other general purpose applications.

3.11 : Seven Segment Display

Q.21 Explain seven segment display in detail.

Ans. : • A display consisting of seven LEDs arranged in seven segments is called seven segment display. It is shown in the Fig. Q.21.1.

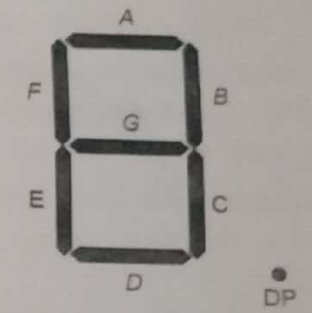


Fig. Q.21.1 Seven segment indicator

• The seven LEDs are arranged in a rectangular fashion and are labeled A through G.

• Each LED is called a **segment** because it forms a part of the digit being displayed. An additional LED is used for the indication of a Decimal Point (DP).

- By forward biasing different LEDs, we can display the digits 0 through 9. For example, to display a zero, the LEDs A, B, C, D, E and F are forward biased.
- Thus in a seven segment display depending upon the digit to be displayed, the particular set of LEDs is forward biased.
- The various digits from 0 to 9 which can be displayed using seven segment display are shown in the Fig. Q.21.2.

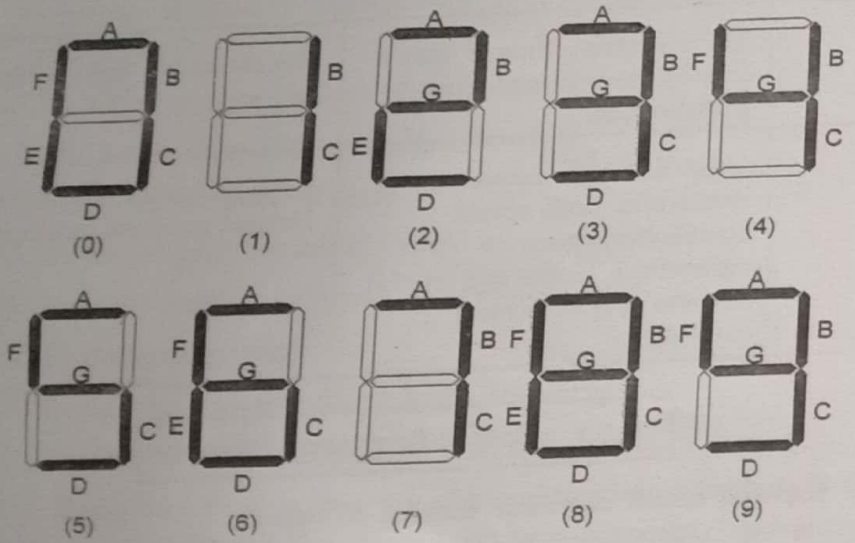


Fig. 21.2 Various digits displayed with 7 segment display

- A seven segment display can also display the capital letters A, C, E and F and also small letters b and d. Microprocessor kits often use such seven segment displays.

Q.22 Explain the two types of seven segment displays.

Ans. : • The two types of seven segment display are available called,

1) Common anode type 2) Common cathode type.

1) Common Anode Type

- In this type, all anodes of LEDs are connected together and common point is connected to + V_{CC} which is positive supply

voltage. A current limiting resistor is required to be connected between each LED and ground. The connection is shown in the Fig. Q.22.1. For the required operation of LEDs, the corresponding cathode is to be connected to the ground.

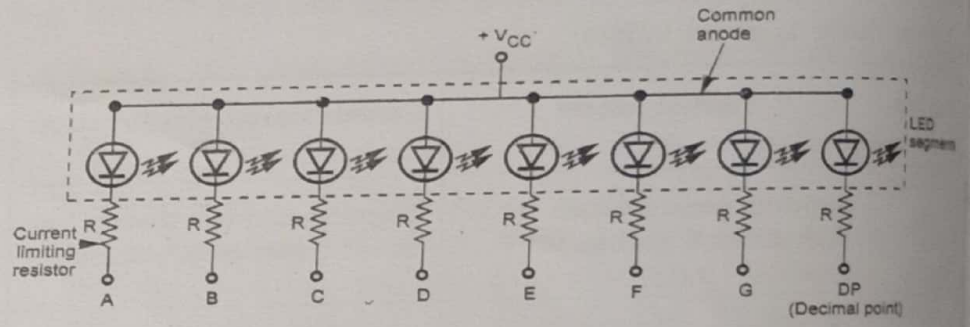


Fig. Q.22.1 Common anode type

2) Common Cathode Type

- In this type, all cathodes of LEDs are connected together and common point is connected to the ground. A current limiting resistor is connected between each LED and the supply + V_{CC}. The anodes of the respective segments are to be connected to + V_{CC} for the required operation of LEDs. The connection of common cathode type display is shown in the Fig. Q.22.2.

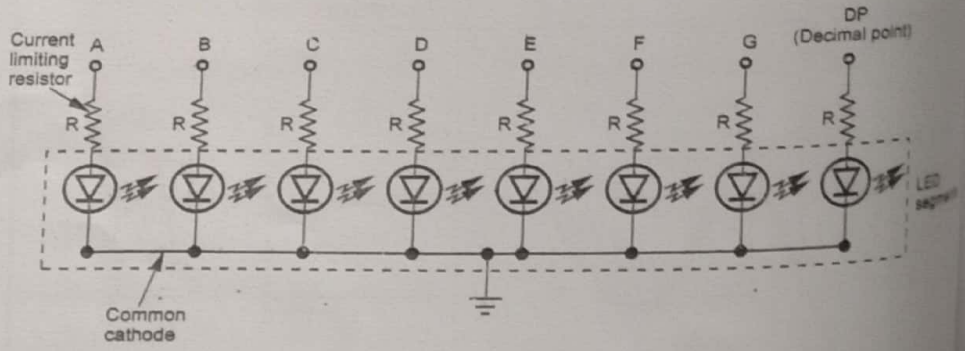


Fig. Q.22.2 Common cathode type

3.12 : Sixteen Segment Display (Alphanumeric Display)

Q.23 Write a note on sixteen segment display.

Ans. : The displays which are used to display alphabets as well as numeric characters in response to the electrical inputs are called sixteen segment displays or alphanumeric displays.

- It consists of 16 segments which are turned on or off according to the required pattern to be produced. The display is shown in the Fig. Q.23.1.

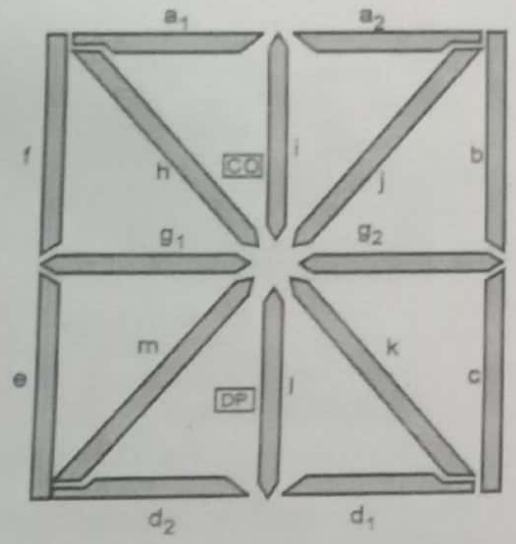


Fig. Q23.1 Sixteen segment display

- Due to diagonally arranged LEDs such as j, h, m, k the characters like, Y, K, M etc. can be displayed.
- The separate vertical LEDs are used for the Decimal Point (DP) and Colon Operator (CO).
- It uses a character generator which translats 7 bit ASCII character codes to the 16 bits which decides which of the 16 segments to turn on or off.
- Alphanumeric LEDs are normally laid out on a single slice of semiconductor material, all the chips being enclosed in a package similar to an IC. The packaging compound is transparent and not opaque.
- The Fig. Q.23.2 shows the display of the characters M and Y.

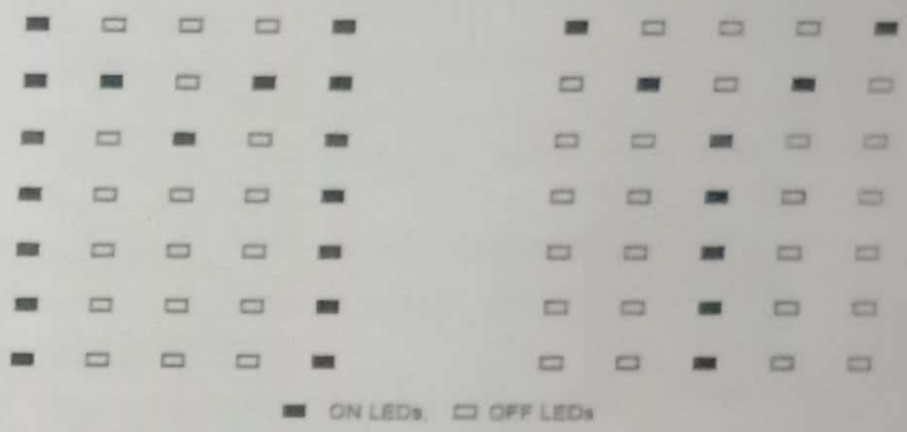


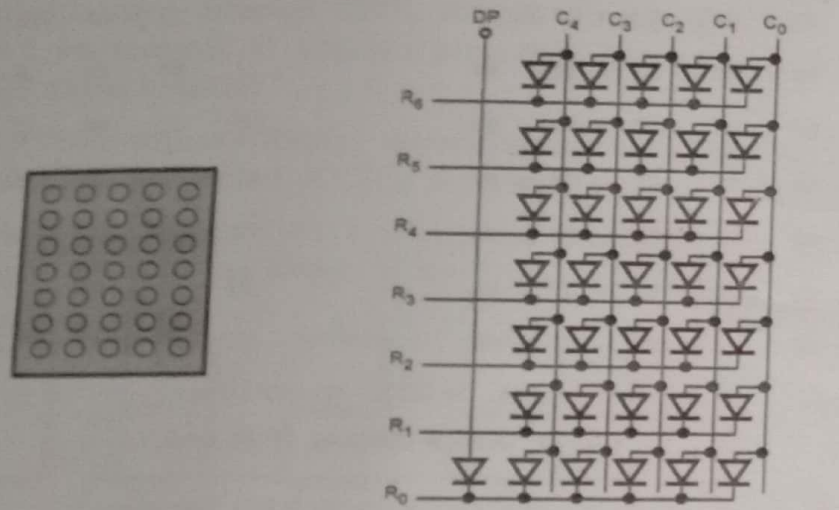
Fig. Q.23.2 Display of M and Y

3.13 : Dot Matrix LED Display

Q.24 What is dot matrix display ? Explain with neat diagram.

Ans. : • In dot matrix displays, arrays of LEDs are used. It uses LED at each dot location in the matrix hence it is called dot matrix display.

- A matrix is formed with the wiring patterns.
- The most commonly used dot matrices are 5 × 7, 5 × 8, 7 × 9. Out of there three patterns, 5 × 7 wiring pattern is most commonly used.
- In 5 × 7 dot matrix display, there are 5 columns and 7 rows of LEDs. The Fig. Q.24.1 shows the 5 × 7 dot matrix display and the circuit connections.
- The wiring pattern may be of common anode or common cathode type.
- Such displays are economical.
- A dot matrix controller converts the instructions from a processor into signals. These signals are used to turn on or off the LEDs of display so that the required pattern is produced.



(a) 5 × 7 dot matrix LED display (b) 5 × 7 dot matrix circuit connections

Fig. Q.24.1

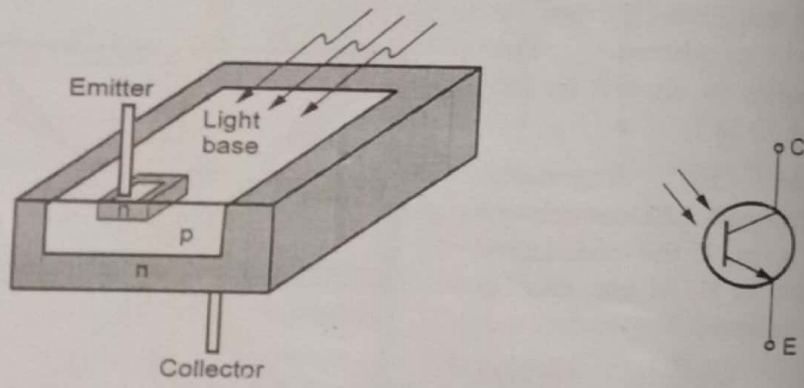
- To improve the brightness of display, a dynamic display system is used. In this, the LEDs are not lit continuously but are sequentially lit by scanning in a "vertical strobe" or "horizontal strobe" mode. This is similar to running lights in modern advertisements.
- In vertical strobe mode, a single row is selected at a time, the appropriate LEDs are energised in that row and then the signal is applied to next row. On the contrary, in horizontal strobe mode, a single column is selected at a time.
- These displays are used to display information on machines, clocks, railway and airplane information displays, watches, calculators etc.

3.14 : Phototransistor

Q.25 Explain the construction, working and characteristics of phototransistor.

Ans. : • A transistor providing internal current multiplication when exposed to light is called phototransistor.

- It has light sensitive collector to base junction. A lens is used so that the base is exposed to the light.
- The base collector area is kept large as it is light sensitive.
- The base terminal is generally not brought out hence phototransistor acts as a two terminal device.
- The construction of a phototransistor is shown in the Fig. Q.25.1 (a) while its symbol is shown in the Fig. Q.25.1 (b).



(a) Construction (b) Symbol

Fig. Q.25.1 Phototransistor

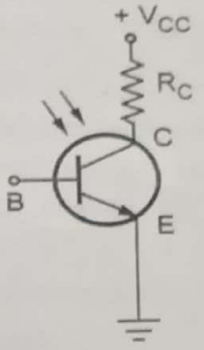
- When no light is incident small leakage current flows from collector to emitter called I_{CEO} due to small thermal generation. This is called **dark current** which is very small of the order of 10^{-9} A.
- When base is exposed to light, base current is produced due to generated electron-hole pairs. This is photocurrent. This is denoted as I_λ.
- This produces collector current which is β times I_λ.

$$\therefore \quad I_C = \beta I_\lambda$$

- The base current I_λ increases as light intensity increases hence collector current also increases with the light intensity.

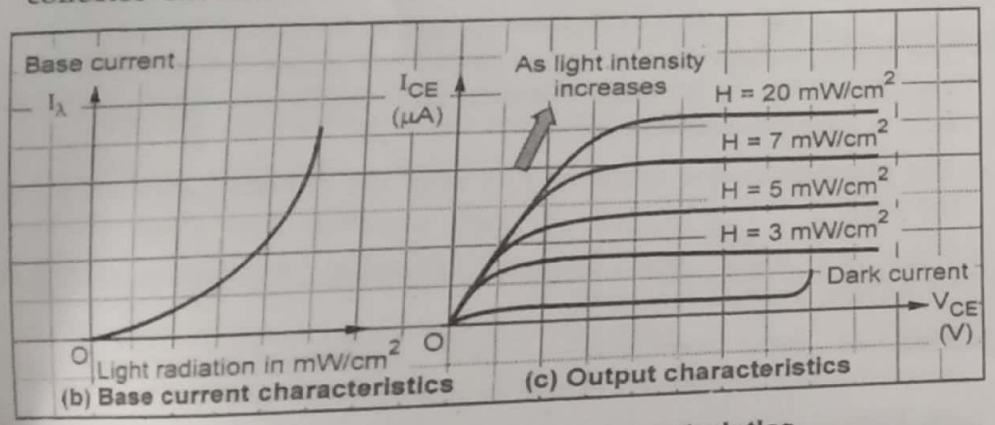
Characteristics

- While biasing phototransistor, the base terminal is kept open.
- The collector is connected to positive of supply through a resistance R_C.
- While the emitter is grounded as shown in the Fig. Q.25.2 (a).
- As light intensity increases, the base current I_λ increases. This is shown in the Fig. Q.25.2 (b).
- The output characteristics are shown in the Fig. Q.25.2 (c) which shows that as the intensity of the light increases (H) then the collector current also increases.



(a) Biasing

Fig. Q.25.2 Phototransistor characteristics



(b) Base current characteristics (c) Output characteristics

Fig. Q.25.2 Phototransistor characteristics

- The phototransistor speed is good but not as fast as photodiode.
- If the base terminal is brought out, the phototransistor can be used as a conventional transistor.

Q.26 State the advantages, disadvantages and applications of phototransistor.

Ans. : Advantages :

1. Higher current production than photodiodes.
2. Works with most visible or near infrared light sources including IREDs, neon bulbs, fluorescent bulbs, incandescent bulbs, lasers, flames, and sunlight
3. Fast-acting with nearly instantaneous output.
4. Relatively inexpensive, simple, and small.

Disadvantages :

1. The material used may limit voltage handling capability.
2. Electrons do not move as freely as they do in electron tubes
3. Vulnerable to electrical surges and electromagnetic energy.
4. The phototransistor speed is good but not as fast as photodiode.

Applications :

1. Monitoring paper position and margin control in printers and copiers
2. Detection in security systems
3. Measuring speed and direction in encoders
4. Remote meter reading for residential electric meters
5. Counting coins or other items
6. Remote controls for audio/visual equipment and appliances
7. Shutter control for cameras
8. Detection for safety shields and other protection systems
9. In level indicators and relays.
10. In computer logic circuits
11. In punch card readers

3.15 : Optocoupler

Q.27 What is optocoupler ? State its types. Explain any one type.

Ans. : • A package which is a combination of light source like LED and a light detector such as photodiode is called an **optocoupler** or **optoisolator**.

• The Fig. Q.27.1 shows the basic construction of LED-photodiode type of optocoupler.

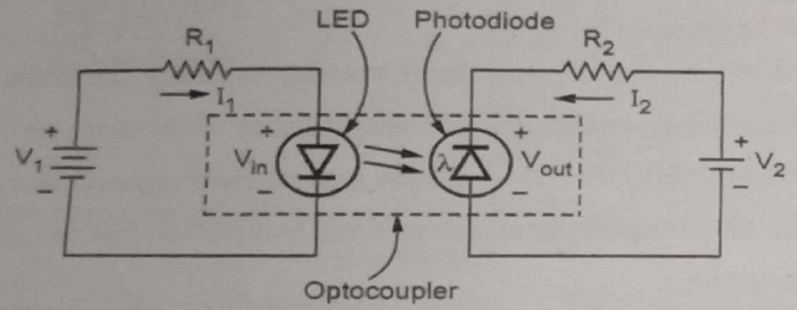


Fig. Q.27.1 LED-photodiode optocoupler

• The LED is forward biased using voltage V_1 and series resistance R_1. The forward current of LED is I_1. Thus LED emits the light.

• The emitted light falls on a photodiode which is reverse biased using a voltage V_2. The reverse current I_2 changes according to the light absorped by the photodiode.

• The output voltage is the difference between the voltage V_2 and the drop across the resistance R_2.

$$\therefore \quad V_{out} = V_2 - I_2 R_2$$

• If the input voltage is changed, the amount of light emitted by LED changes. This changes the reverse current of the photodiode. Hence the output voltage changes.

• The output voltage is optically coupled with the input voltage, though electrically isolated. Thus the deviced couples input circuit to output circuit optically hence called optocoupler or optoisolator.

• The various types of optocouplers are,

1. LED - LDR (Light Dependent Resistor) optocoupler
2. LED - photodiode optocoupler
3. LED - phototransistor optocoupler.

LED - Phototransistor Optocoupler

• The Fig. Q.27.2 shows LED - phototransistor optocoupler.

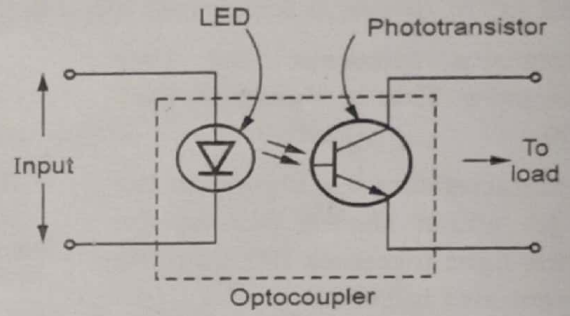


Fig. Q.27.2 LED-phototransistor optocoupler

• The input voltage and a series resistance is used to forward bias the LED. Due to forward current, LED emits the light. The light falls on the phototransistor.

• The phototransistor becomes ON and the resulting current drives the load.

• Thus the input gets optically coupled to the output load providing electric isolation.

• This is very commonly used optocoupler as additional amplification of current is not required.

Q.28 Define and explain the various characteristics of optocoupler.

Ans. : • The various characteristics of optocoupler are,

1. **Current transfer ratio (CTR) :** It is the ratio of output collector current (I_C) to the input forward current (I_F).
2. **Isolation voltage between input and output (V_{iso}) :** This is important as optocouplers are used to transmit signals from one circuit to another which are having different potentials. It is specified in KV_{rms}.

3. **Response time :** It indicates how fast the optocoupler can change its state. It depends on output phototransistor.

4. **Common mode rejection :** Though optocouplers provide electric isolation, for low frequency signal, a common noise can appear at the output due to stray capacitance. The common mode rejection indicates the ability of the optocoupler to reject such common mode signals. Its value must be high.

Q.29 State the advantages and applications of optocoupler.

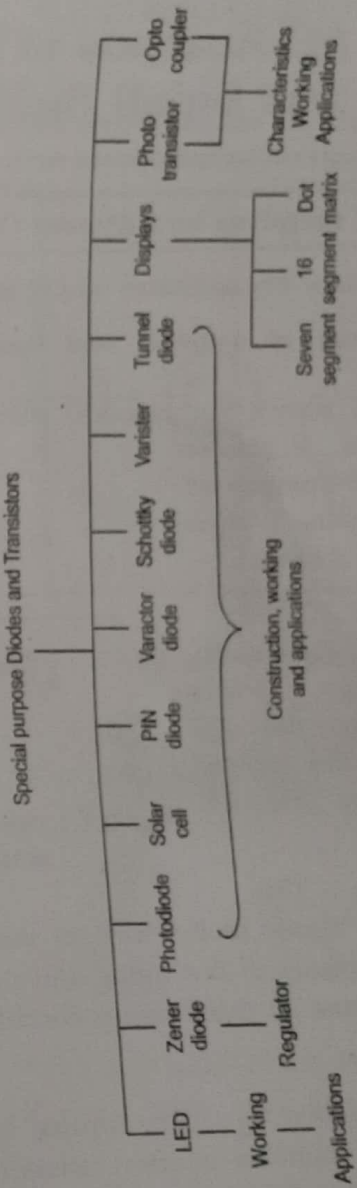
Ans. : • The various advantages of optocoupler are,

1. Provides electric isolation between input and output.
2. The response time is very small hence operation is fast.
3. Capable of wideband signal transmission.
4. Due to unidirectional signal transfer, the output does not loop back to the input.
5. Easy interfacing with logic devices.
6. Compact and light weight.
7. Changing load, does not affect the input.
8. The problems such as noise, contact bounce etc. are eliminated.
9. No moving parts hence less maintenance.

• The various applications of optocouplers are,

1. Mostly used for high voltage applications due to electric isolation.
2. Interfacing the output of computer to external electric circuit.
3. In driving the motors, relays, buzzers, alarms etc.
4. In a.c. to d.c. converters used for d.c. motor speed control.
5. In high power choppers and inverters.

Memory Map



END...

4 AC Analysis of BJT Circuits and Small Signal Amplifier

4.1 Coupling and Bypass Capacitors

Q.1 Draw and explain the operation of CE amplifier.

OR Explain the use of coupling and bypass capacitors in CE amplifier.

Ans. : • Fig. Q.1.1 shows the practical circuit of common emitter transistor amplifier. It consists of different circuit component. The functions of these components are as follows :

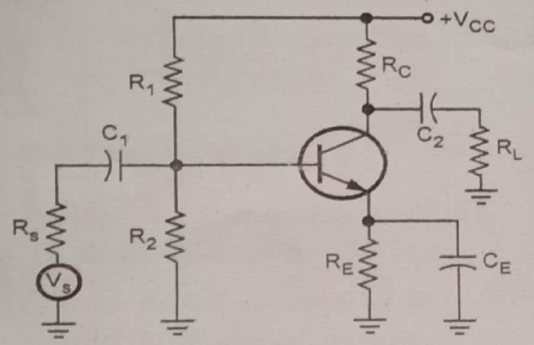


Fig. Q.1.1 Practical common emitter amplifier circuit

1. Biasing Circuit :
The resistances R_1, R_2 and R_E forms the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.

2. Input Capacitor C_1 : This capacitor couples the signal to the base of the transistor. It blocks any d.c. component present in the signal and passes only a.c. signal for amplification. Because of this biasing conditions are maintained constant.

3. Emitter Bypass Capacitor C_E : An emitter bypass capacitor C_E is connected in parallel with the emitter resistance, R_E to provide a low reactance path to the amplified a.c. signal. If it is not inserted, the amplified a.c. signal passing through R_E will cause a voltage

drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. Output Coupling Capacitor C_2 : The coupling capacitor C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks d.c. and passes only a.c. part of the amplified signal.

Q.2 Explain the need for C_1, C_2 and CE in detail.

Ans. : • We know that, the impedance of capacitor is given as,

$$X_C = \frac{1}{2\pi fC}$$

- Thus, at signal frequencies all the capacitors have extremely small impedance and it can be treated as an a.c. short circuit. For bias/d.c. conditions of the transistor all the capacitors act as a d.c. open circuit. With this knowledge we will see the importance of C_1, C_2 and C_E.
- Consider that the signal source is connected directly to the base of the transistor as shown in Fig. Q.2.1.

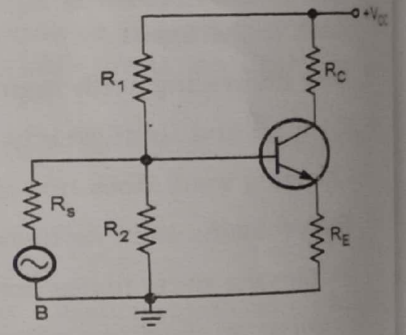


Fig. Q.2.1

- Looking at the Fig. Q.2.1 we can immediately notice that source resistance R_s is in parallel with R_2. This will reduce the bias voltage at the transistor base and, consequently alter the collector current, which is not desired. Similarly, by connecting R_L directly, the d.c. levels of V_C and V_E will change. To avoid this and maintain the stability of bias condition coupling capacitors are connected. As mentioned earlier, coupling capacitors act as open circuits to d.c., maintaining stable biasing conditions even after connection of R_s and R_L. Another advantage of connecting C_1 is that any d.c. component in the signal is opposed and only a.c. signal is routed to the transistor amplifier.

- The emitter resistance R_E is one of the component which provides bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor C_E provides a low reactance path to the amplified a.c. signal increasing the output voltage swing.

Q.3 What is AC degeneration ?

Ans. : • In collector to base bias circuit, the voltage change at the transistor collector (produced by the ac input) is fedback to the base, where it tends to partially cancel the signal. This effect is known as ac degeneration and it can result in a very low voltage gain.

Q.4 Comment on capacitor polarity.

Ans. : • For the proper operation of the circuit, polarities of the capacitors must be connected correctly. The curve bar which indicates negative terminal must always be connected at a d.c. voltage level lower than (or equal to) the d.c. level of the positive terminal (straight bar).

Q.5 Explain the way to eliminate the effect of ac degeneration in collector to base bias circuit.

Ans. : • Fig. Q.5.1 shows how ac degeneration is eliminated in collector to base bias circuit. Here, R_B is replaced by two equal resistors R_{B1} and R_{B2} and a bypass capacitor is connected from the junction of R_{B1} and R_{B2} to the ground terminal.

- Capacitor C_B offers a short circuit to ac signals, so that there is no feedback from the transistor collector to the base.

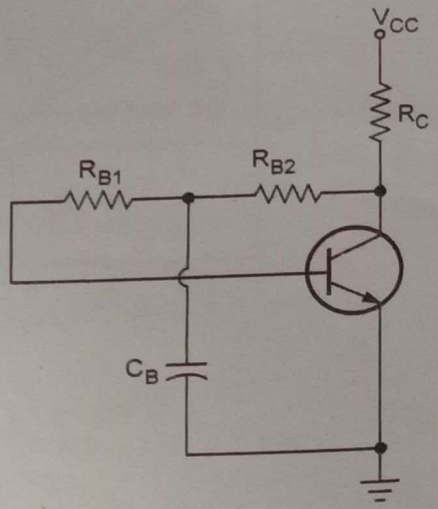


Fig. Q.5.1

4.2 AC Load Lines

Q.6 What is ac load line ?

Ans. : • Fig. Q.6.1 (a) and (b) show the CE amplifier circuit with voltage divider bias and its ac equivalent circuit.

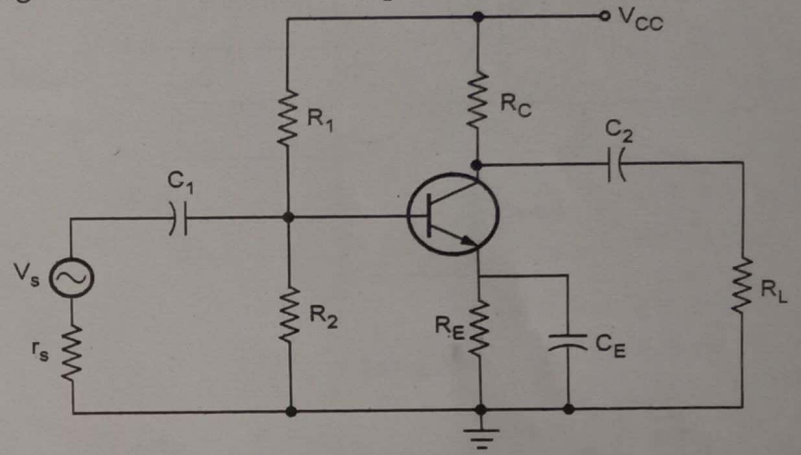


Fig. Q.6.1 (a) CE amplifier circuit

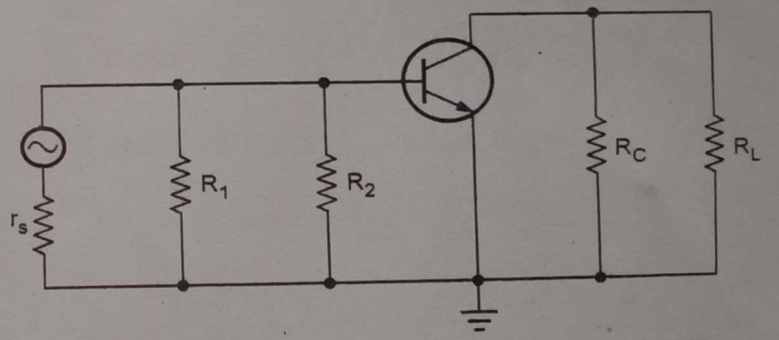


Fig. Q.6.1 (b) ac equivalent of CE amplifier circuit

- The dc load for the circuit is $R_C + R_E$. On the other hand ac load for the circuit is $R_C || R_L$.
- It is important to note that effective ac load is always less than effective dc load. Therefore, the slope of the ac load line is always higher than the dc load line.

Q.7 Draw the dc and ac load lines for the transistor circuit shown in Fig. Q.7.1.

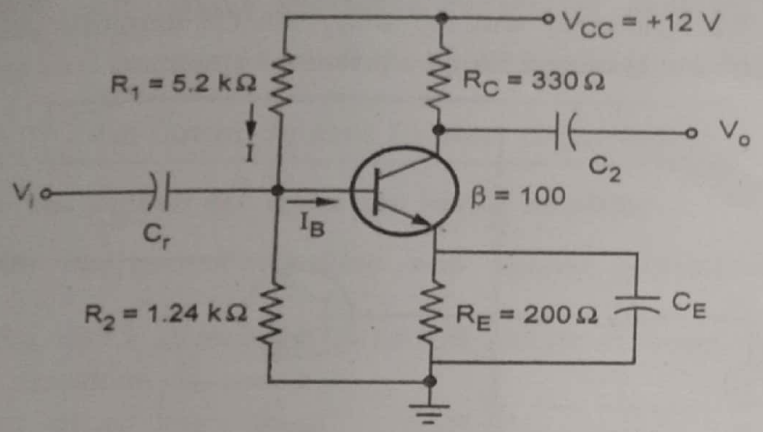


Fig. Q.7.1

Ans. : DC load line

- Since, βR_E = 20 K and which is greater than 10 R_2 we can use approximate analysis.

$$V_B = \frac{V_{CC}R_2}{R_1+R_2} = \frac{12\times1.24}{5.2+1.24} = \mathbf{2.31\ V}$$

$$V_E = V_B - V_{BE} = 2.31 - 0.7 = \mathbf{1.61\ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.61}{200} = \mathbf{8\ mA}$$

$$I_B = \frac{I_E}{1+\beta} = \frac{8\ mA}{1+100} = \mathbf{79.2\ \mu A}$$

$$I_C = \beta I_B = 100\times79.2\ \mu A = 7.92\ mA$$

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$= 12 - 7.92\times10^{-3}\times330 - 1.61 = \mathbf{7.776\ V}$$

AC load line

Since there is no R_L,

$$R_{L(ac)} = R_C = 330\ \Omega$$

where I_C changes by ΔI_C = 7.92 mA,

$$\Delta V_{CE} = \Delta I_C \times R_C$$

$$= 7.92\ mA \times 330\ \Omega$$

$$= \mathbf{2.614\ V}$$

- Plotting point C at ΔI_C = 7.92 mA and ΔV_{CE} = 2.614 V from the Q-point, we can draw the ac load line through points C and Q.

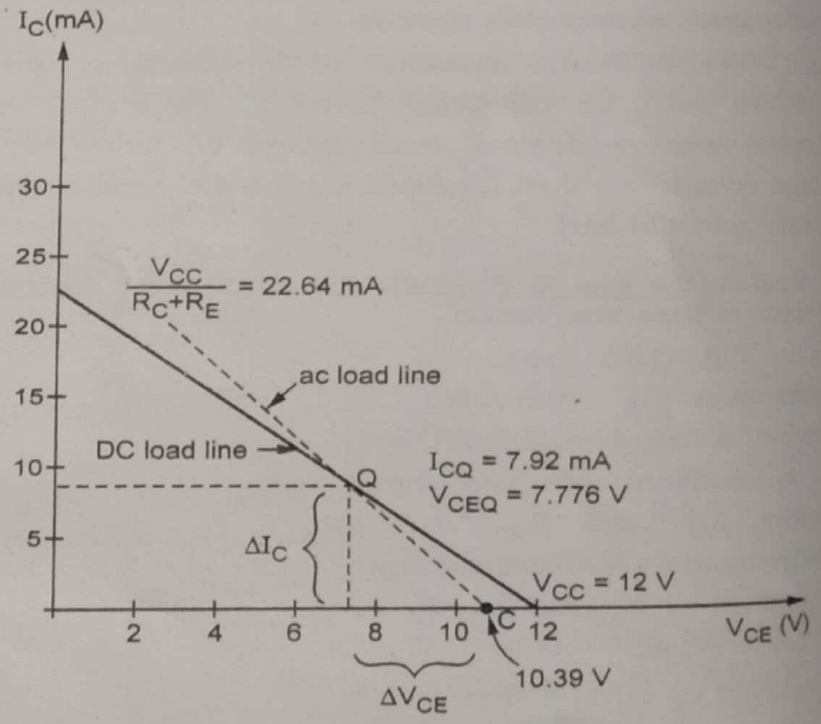


Fig. Q.7.2 dc and ac load lines

aw the dc and ac load lines for the transistor circuit shown Q.7.1.

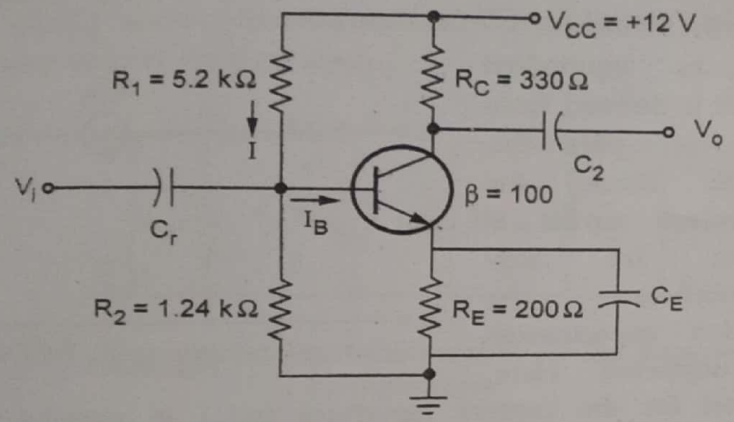


Fig. Q.7.1

Ans. : DC load line

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$$V_E = V_B - V_{BE} = 2.31 - 0.7 = \mathbf{1.61\ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.61}{200} = \mathbf{8\ mA}$$

$$I_B = \frac{I_E}{1+\beta} = \frac{8\ mA}{1+100} = \mathbf{79.2\ \mu A}$$

$$I_C = \beta I_B = 100\times79.2\ \mu A = 7.92\ mA$$

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$$= 12 - 7.92\times10^{-3}\times330 - 1.61 = \mathbf{7.776\ V}$$

AC load line

Since there is no R_L,

$$R_{L(ac)} = R_C = 330\ \Omega$$

where I_C changes by ΔI_C = 7.92 mA,

$$\Delta V_{CE} = \Delta I_C \times R_C$$

$$= 7.92\ mA \times 330\ \Omega$$

$$= \mathbf{2.614\ V}$$

- Plotting point C at ΔI_C = 7.92 mA and ΔV_{CE} = 2.614 V from the Q-point, we can draw the ac load line through points C and Q.

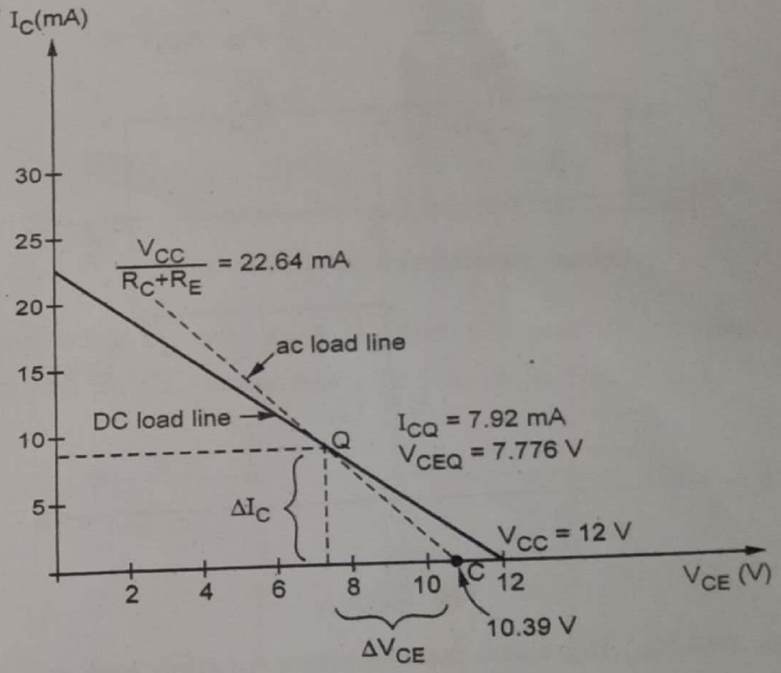


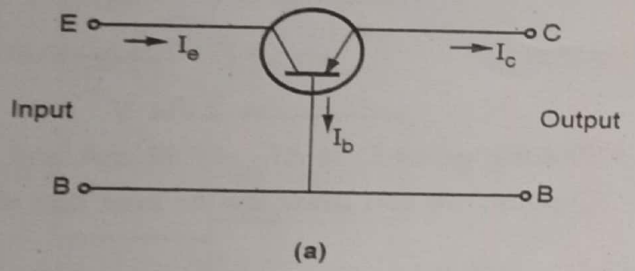
Fig. Q.7.2 dc and ac load lines

4.3 Transistor Models and Parameters

Q.8 Draw and explain the T-equivalent and r-parameter model for common base configuration.

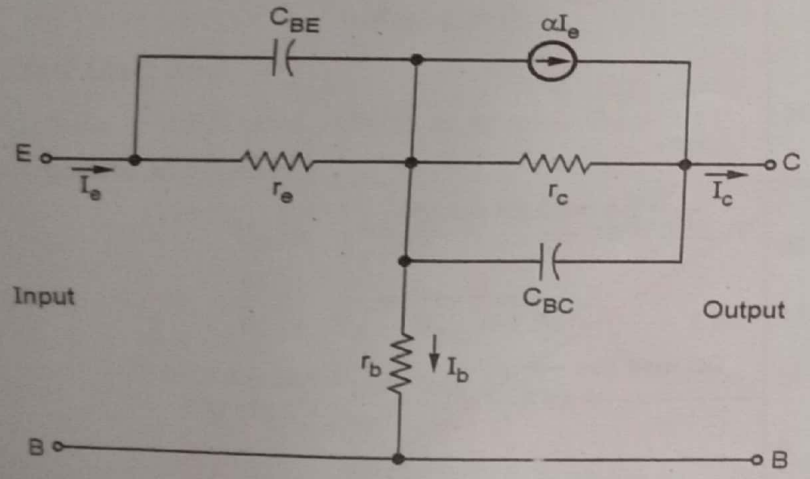
Ans. : • Fig. Q.8.1 show the T equivalent circuit or r-parameter equivalent circuit for a transistor in CB configuration.

• Here, resistor r_e represents the BE junction resistance, r_c represents the CB junction resistance, and r_b represents the resistance of the base region.



(a)

Fig. Q.8.1



(b)

Fig. Q.8.1

• The C_{BE} and C_{BC} represent the respective junction capacitances.

• The current generator connected in parallel with r_c and C_{BC}, represents the collector current following out of the collector terminal. It is represented by αI_e (where $\alpha = I_c / I_e$).

Q.9 Draw and explain the transistor low frequency r-parameter ac equivalent circuit for CB configuration.

Ans. : • Fig. Q.9.1 shows the low frequency r-parameter ac equivalent circuit for CB configuration.

• The ac equivalent circuit is derived from the r-parameter model. Since, the equivalent circuit is drawn for low frequencies, the junction capacitances are neglected. Here, instead for the current generator (αI_e) in parallel with r_c, voltage generator ($\alpha I_e r_c$) is connected in series with r_c.

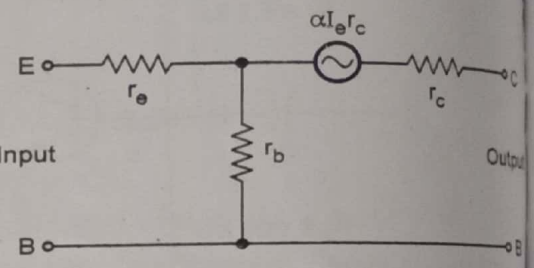


Fig. Q.9.1

$$r_e = \frac{\Delta V_{BE}}{\Delta I_E}$$

The ac resistance for the transistor BE junction can be calculated as

$$r_e' = \frac{26\,mV}{I_E}$$

Q.10 Draw and explain the h-parameter model for the CE configuration.

Ans. : • To see how we can derive a hybrid model for a transistor, let us consider the common emitter configuration shown in Fig. Q.10.1. The variables I_b, I_c, V_b and V_c represent total instantaneous currents and voltages.

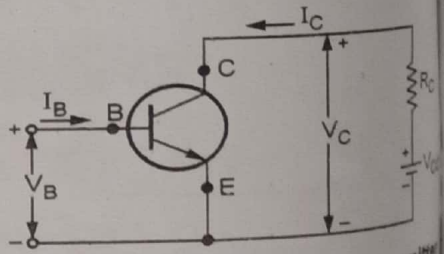


Fig. Q.10.1 Simple common emitter configuration

I_b = Input current

I_c = Output current

V_{be} = Input voltage

V_{ce} = Output voltage

- Fig. Q.10.2 shows the h-parameter equivalent circuit for the common emitter configuration.

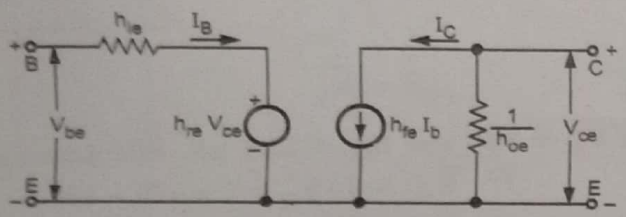


Fig. Q.10.2 h-parameter equivalent circuit for the common emitter configuration

- From the h-parameter equivalent circuit of the common emitter configuration we can write,

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \quad \ldots (1)$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \quad \ldots (2)$$

where

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} \text{ constant}} \quad \ldots (3)$$

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B \text{ constant}} \quad \ldots (4)$$

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} \text{ constant}} \quad \ldots (5)$$

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right|_{I_B \text{ constant}} \quad \ldots (6)$$

- The quantities ΔV_{BE} (V_{be}), ΔV_{CE} (V_{ce}), ΔI_B (I_b) and ΔI_C (I_c) represent the small change in base and collector voltages and currents.
- Here, h_{ie} represents input resistance, $h_{re} V_{ce}$ represents the feedback voltage as the portion h_{re} of the output voltage V_{ce}, h_{re} represents reverse voltage transfer ratio and $1/h_{oe}$ represents device output resistance.

Q.11 Draw and explain the approximate h-parameter model for CE configuration and derive r_π model from it.

Ans. : • Fig. Q.11.1 shows the approximate h-parameter model for CE configuration. Here, $h_{re} V_{ce}$ (Feedback generator) is neglected.

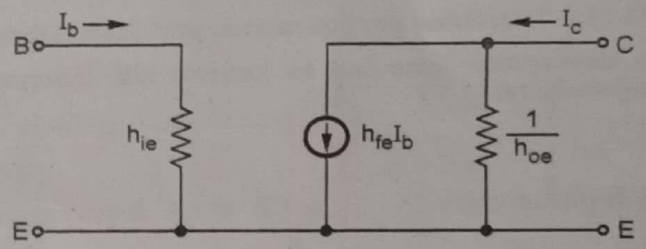


Fig. Q.11.1 CE h-parameter model

- By replacing h_{ie} with r_π, $h_{fe} I_b$ with βI_b and $1/h_{oe}$ by r_c we have r_π model for CE configuration as shown in Fig. Q.11.2.

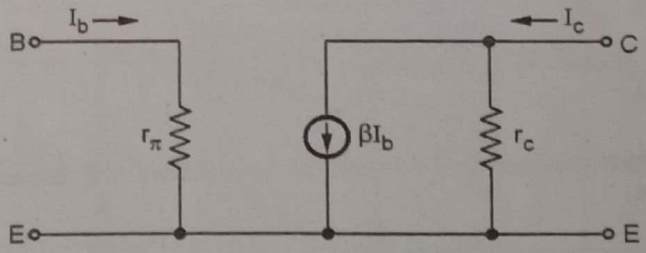


Fig. Q.11.2 CE r_π transistor model

Q.12 Draw the h-parameter model for CB and CC configurations.

Ans. :

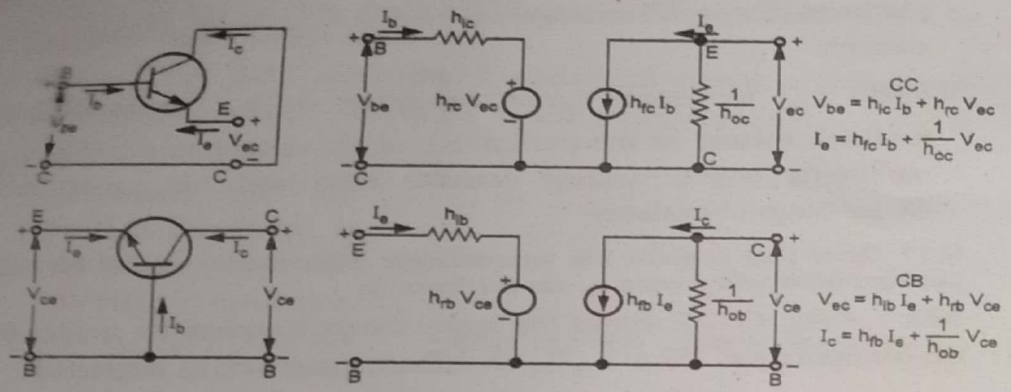


Fig. Q.12.1 Transistor configurations and their hybrid models

Q.13 Give conversion formulae to convert CE h-parameter to CB and CC h-parameters.

Ans. :

CE to CB h-parameters	CE to CC h-parameters
$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	$h_{ic} = h_{ie}$
$h_{rb} = \frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re}$
$h_{fb} = \frac{h_{fe}}{1+h_{fe}}$	$h_{fc} = 1 + h_{fe}$
$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{oo} = h_{oe}$

Q.14 Give the conversion formulae to convert CE h-parameters to r-parameters.

Ans. :

$$\alpha = \frac{h_{fe}}{1+h_{fe}}$$

$$r_c = \frac{1+h_{fe}}{h_{oe}}$$

$$r_e = \frac{h_{ie}}{1+h_{fe}} = r'_e$$

$$r_b = h_{ie} - \frac{h_{re}(1+h_{fe})}{h_{oe}}$$

$$r_\pi = h_{ie}$$

$$\beta = h_{fe}$$

Q.15 For $h_{fe} = 120$ and $h_{oe} = 12.1\ \mu S$, calculate h_{fc}, h_{ob} and α.

Ans. :

$$h_{fc} = 1 + h_{fe} = 1 + 120 = 121$$

$$h_{ob} \approx \frac{h_{oe}}{1+h_{fe}} = \frac{12.1\mu S}{1+120} = 100\ \mu S$$

$$\alpha \approx \frac{h_{fe}}{1+h_{fe}} = \frac{120}{1+120} = 0.992$$

Q.16 For a transistor, $I_B = 20\ \mu A$ and $I_c = 1$ mA. Calculate r'_e, r_π and β.

Ans. :

$$r'_e = \frac{26\ mV}{I_E} = \frac{26\ mV}{1.02\ mA} = 25.49\ \Omega$$

$$h_{fe} = \frac{I_C}{I_B} = \frac{1\ mA}{20\ \mu A} = 50$$

$$h_{ie} = (1+h_{fe}) r'_e = (1 + 50) \times 25.49$$

$$= 1.3\ k\Omega$$

$$r_\pi = h_{ie} = 1.3\ k\Omega$$

$$\beta = h_{fe} = 50$$

4.4 Common Emitter Circuit Analysis

Q.17 Draw and explain the operation of CE amplifier circuit with neat waveform.

Ans. : • Fig. Q.17.1 shows the common emitter (CE) amplifier circuit.

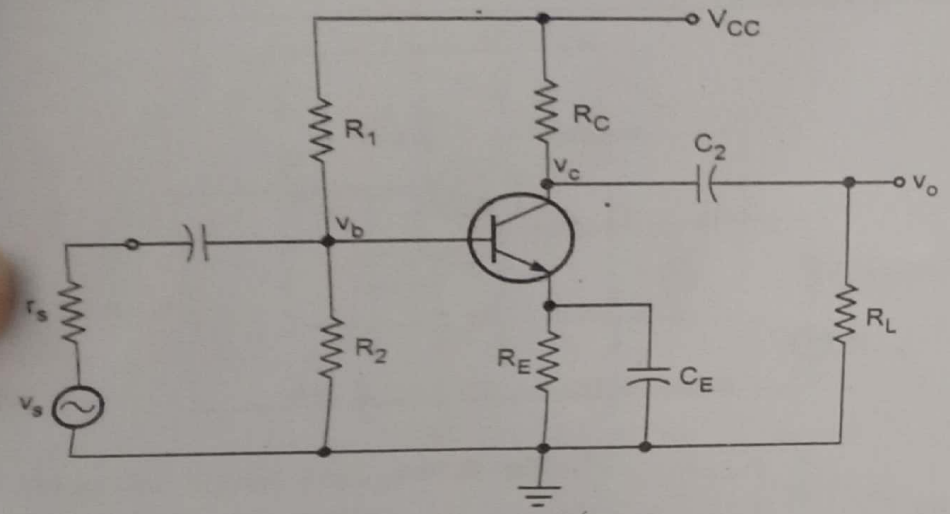


Fig. Q.17.1 CE amplifier

Here, input is applied to the base via C_1. When v_s increases in a positive direction, it increase the V_{BE}. The increase in V_{BE} raises the level of I_c, thereby increasing the voltage drop across R_C and thus reducing the level of the collector voltage (V_C). The change in V_C is capacitor coupled to the circuit output to produce ac output voltage (v_o).

It seen that as v_s increases in positive direction, v_o goes in a negative direction and when v_s changes in a negative direction, v_o goes in positive direction. Thus we can say that there is a 180° phase shift between input and output waveforms.

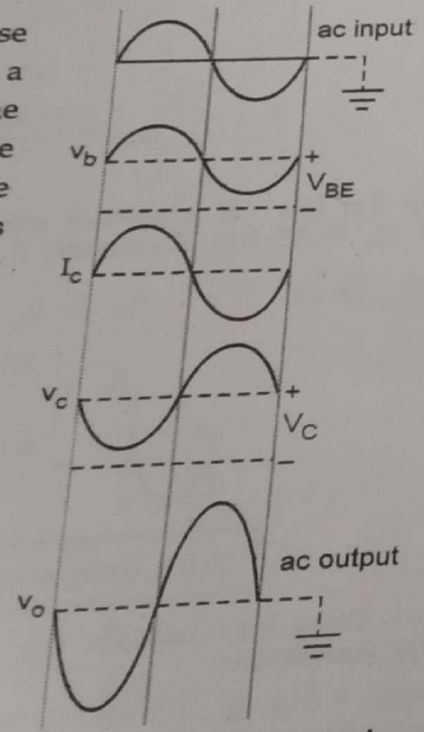


Fig. Q.17.2 Voltage and current waveform in CE

Q.18 Derive the expressions for input impedance, output impedance, voltage gain, current gain and power gain for common emitter circuit.

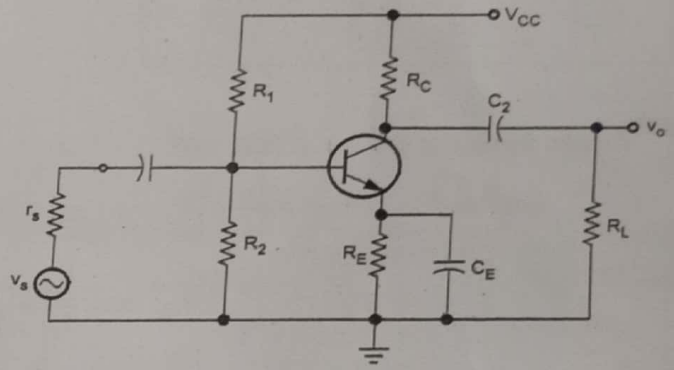
Ans. : • Fig. Q.18.1 (a) and (b) shows the common emitter circuit and its h-parameter equivalent circuit.

Input impedance : $Z_b = h_{ie}$

Overall input impedance : $Z_i = R_1 || R_2 || h_{ie}$

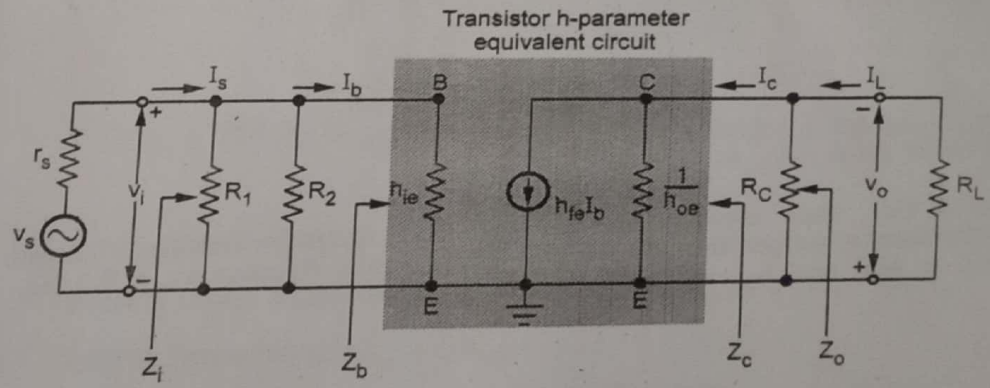
Output impedance : $Z_c = \frac{1}{h_{oe}}$

Overall output impedance = $Z_o = R_c || \frac{1}{h_{oe}}$



(a) CE amplifier

Fig. Q.18.1



(b) h-parameter equivalent circuit

Fig. Q.18.1

Voltage gain :

$$A_v = \frac{v_o}{v_i} = \frac{-I_c(R_C||R_L)}{I_b h_{ie}}$$

$$= \frac{-h_{fe}(R_C||R_L)}{h_{ie}} \qquad \because \frac{I_c}{I_b} = h_{fe}$$

Note : Minus sign indicates that v_o is 180° out of phase with v_i

$$A_v = \frac{-h_{fe}(R_C||R_L)}{h_{ie}} \approx \frac{-(1+h_{fe})(R_C||R_L)}{h_{ie}} \qquad \because h_{fe} >> 1$$

$$= \frac{-(R_C||R_L)}{h_{ib}} \qquad \because h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

$$= \frac{-(R_C||R_L)}{r_e'} \qquad \because h_{ib} = r_e'$$

Current gain :

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

where $\frac{I_L}{I_s} = \frac{-R_C}{R_C+R_L}$, $\frac{I_c}{I_b} = h_{fe}$ and $\frac{I_b}{I_s} = \frac{R_B}{R_B+Z_i}$

$$R_B = R_1||R_2$$

$$A_i = \frac{-R_C}{R_C+R_L} \times h_{fe} \times \frac{R_B}{R_B+h_{ie}}$$

$$= \frac{-h_{fe} R_C R_B}{(R_C+R_L)(R_B+h_{ie})}$$

Power gain : $A_p = A_v \times A_i$

Q.19 For the circuit shown in Fig. Q.19.1 calculate input impedance, output impedance and voltage gain. Assume h_{ie} = 2.1 kΩ, h_{fe} = 100 and h_{oe} = 1 μS

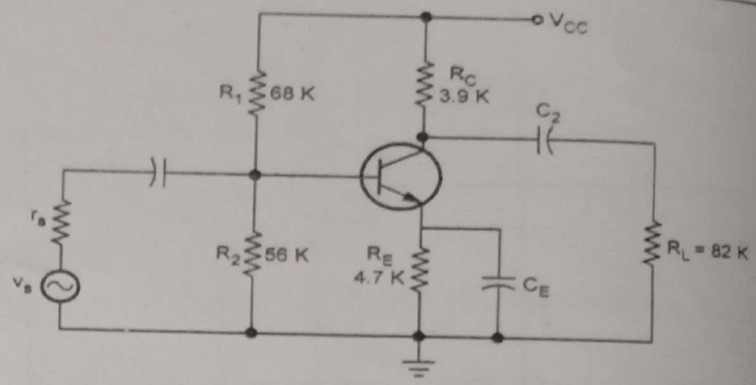


Fig. Q.19.1

Ans. :

$$Z_i = R_1||R_2||h_{ie} = 68\,K||56\,K||2.1\,K = 1.97\,k\Omega$$

$$Z_o = R_C||(1/h_{oe}) = 3.9\,K\,||\,(1/1\mu S)$$

$$\approx 3.9\,k\Omega$$

$$A_v = \frac{-h_{fe}(R_C||R_L)}{h_{ie}} = \frac{-100(3.9\,||\,82)}{2.1} = -177.28$$

Q.20 For the CE amplifier circuit, if I_C = 1.5 mA, R_C = 3.3 kΩ and R_L = 33 kΩ. Calculate r_e' and the voltage gain.

Ans. : Since $I_E \approx I_C$ we have

$$r_e' \approx \frac{26\,mV}{J_C} \approx \frac{26\,mV}{1.5\,mA} = 17.33\,\Omega$$

$$A_v = \frac{-(R_C\,||\,R_C)}{r_e'} = \frac{-(3.3\,K||33\,K)}{17.33} = -173.11$$

4.5 : Common Base Circuit Analysis

Q.21 Draw and explain the operation of CB amplifier circuit with neat waveforms.

Ans. : • Fig. Q.21.1 shows the common base (CB) amplifier circuit. Here, input is applied to the emitter via C_2, there is no bypass capacitor, base terminal is ac grounded via C_1 and the output voltage is developed across R_C.

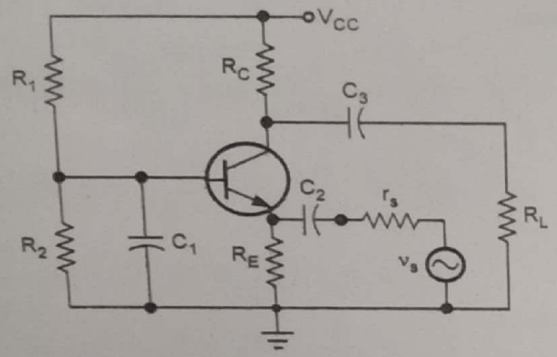


Fig. Q.21.1 CB amplifier circuit

- Since, the signal voltage is applied at emitter terminal, positive - going signal reduces the base - emitter voltage. Reduction in V_{BE} reduces collector current and increases voltage at collector (v_C). Rise in v_C is effectively a rise in the circuit output voltage (v_O). A positive going input signal produces positive - going output. Similarly, negative - going input signal produces negative - going output and there is no phase - shift between input and output.

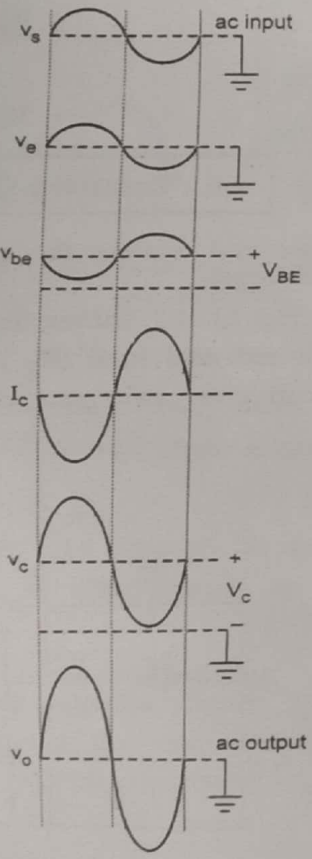


Fig. Q.21.2 Voltage and current waveforms for CB amplifier circuit

Q.22 Derive the expressions for input impedance, output impedance and voltage gain for common base circuit.

Ans. : Fig. Q.22.1 (a) and (b) shows the common base amplifier circuit and its h - parameter equivalent circuit.

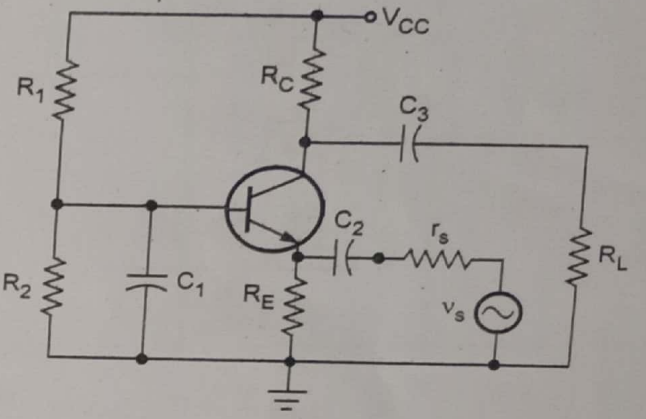


Fig. Q.22.1 (a) CB amplifier circuit

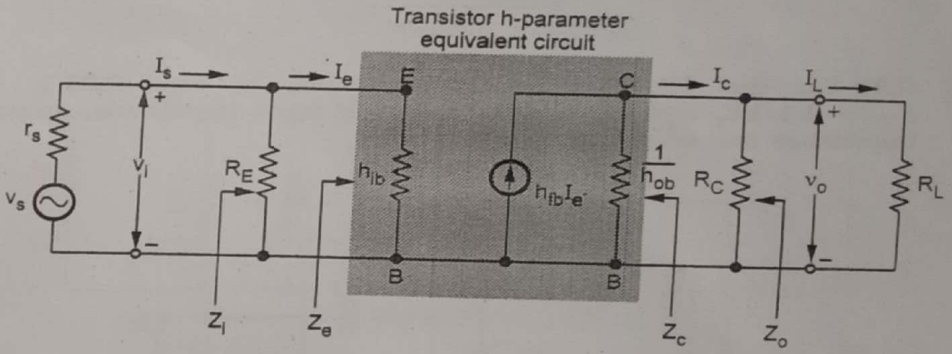


Fig. Q.22.1 (b) h - parameter equivalent circuit for CB amplifier

Input impedance : $Z_e = h_{ib}$

Overall input impedance : $Z_i = Z_e \,||\, R_E = Z_e \quad \because R_E >> Z_e$

Output impedance : $Z_c = 1/h_{ob}$

Overall output impedance : $Z_o = Z_c \,||\, R_C = R_C \quad \because Z_c >> R_C$

Voltage gain : $A_v = \frac{v_o}{v_i}$

$$= \frac{h_{fb} I_c (R_C \| R_L)}{I_e h_{ib}}$$

$$= \frac{h_{fb} I_e (R_C \| R_L)}{I_e h_{ib}} \qquad \because I_c = I_E$$

$$\therefore A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib}}$$

$$= \frac{\left(\frac{h_{fe}}{1+h_{fe}}\right)(R_C \| R_L)}{\frac{h_{ie}}{1+h_{fe}}} \qquad \because h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

and $h_{fb} = \frac{h_{fe}}{1+h_{fe}}$

$$= \frac{h_{fe}(R_C \| R_L)}{h_{ie}}$$

Q.23 For the CB amplifier circuit shown in Fig. Q.23.1, if h_{ie} = 2.1 kΩ and h_{fe} = 100, calculate input impedance, output impedance and voltage gain.

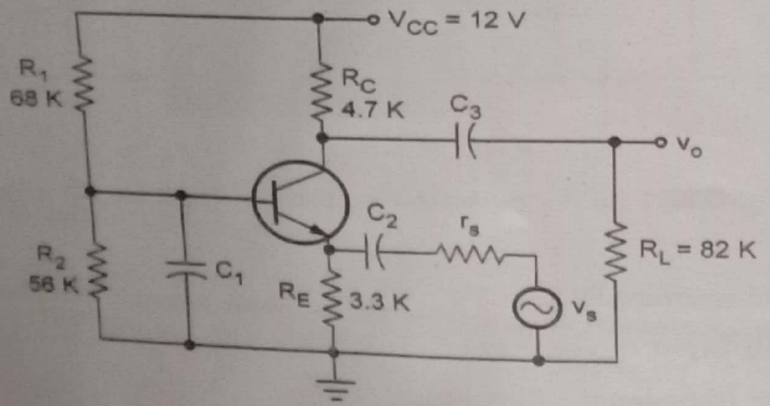


Fig. Q.23.1

Ans. : We have,

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}} = \frac{2.1\ k\Omega}{1+100} = \mathbf{20.79\ \Omega}$$

$$h_{fb} = \frac{h_{fe}}{1+h_{fe}} = \frac{100}{1+100} = \mathbf{0.99}$$

$$Z_i = h_{ib} \| R_E = 20.79 \| 3.3\,K = \mathbf{20.66\ \Omega}$$

$$Z_o = \frac{1}{h_{ob}} \| R_C \approx R_C = \mathbf{4.7\ K}$$

$$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib}} = \frac{0.99(4.7K \| 82K)}{20.79}$$

$$= \mathbf{211.68}$$

4.6 : Common Collector Circuit Analysis

Q.24 Draw and explain the operation of CC amplifier circuit with neat waveforms.

Ans. : • Fig. Q.24.1 shows the common base (CC) amplifier circuit. Here, the external load (R_L) is capacitor - coupled to the emitter. The circuit uses voltage - divider bias to provide DC bias. The

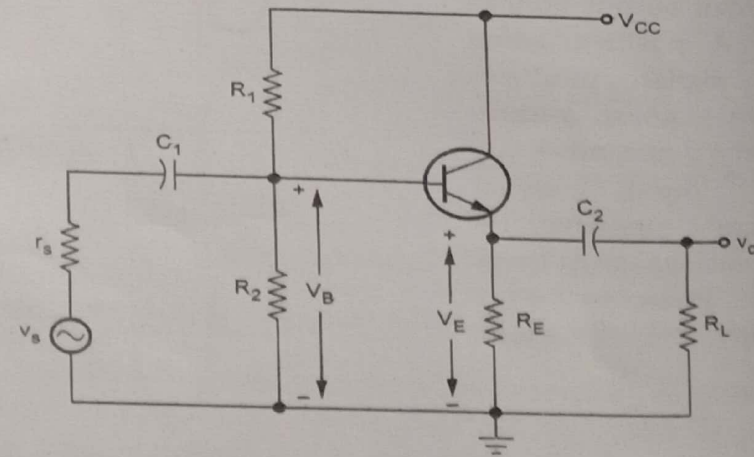


Fig. Q.24.1 CC amplifier circuit

cuit output voltage is veloped across the emitter esistance and there is no bypass capacitor.

- We know that $V_B = \frac{V_{CC}R_2}{R_1 + R_2}$ and $V_E = V_B - V_{BE}$. When signal is applied via C_1 to the base of the transistor, V_B increases and decreases as the signal goes positive and negative.
- Since, V_{BE} is substantially constant, changes appeared in the V_B also appears in the V_E. The change in V_E is coupled via C_2 to give an ac output voltage.

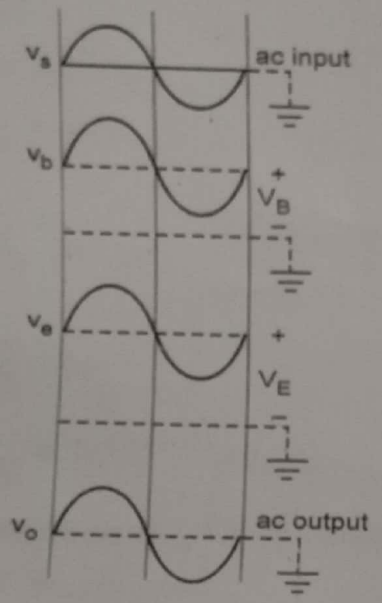


Fig. Q.24.2 Voltage waveforms for CC amplifier

- It is seen that the ac output voltage from a CC amplifier circuit is essentially the same as the input voltage and there is no voltage gain or phase shift.
- Since, the CC output voltage follows the changes in the signal voltages, the CC amplifier circuit is also known as **emitter follower.**

Q.25 Derive the expressions for input impedance, output impedance and voltage gain for common collector circuit.

Ans. : • Fig. Q.25.1 (a) and (b) shows the common collector amplifier circuit and its h - parameter equivalent circuit.

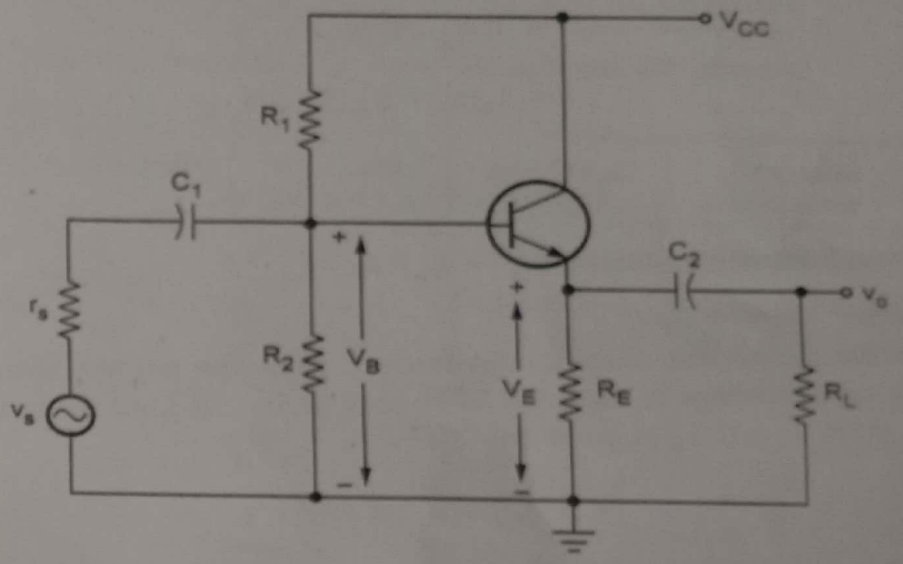


Fig. Q.25.1 (a) CC amplifier circuit

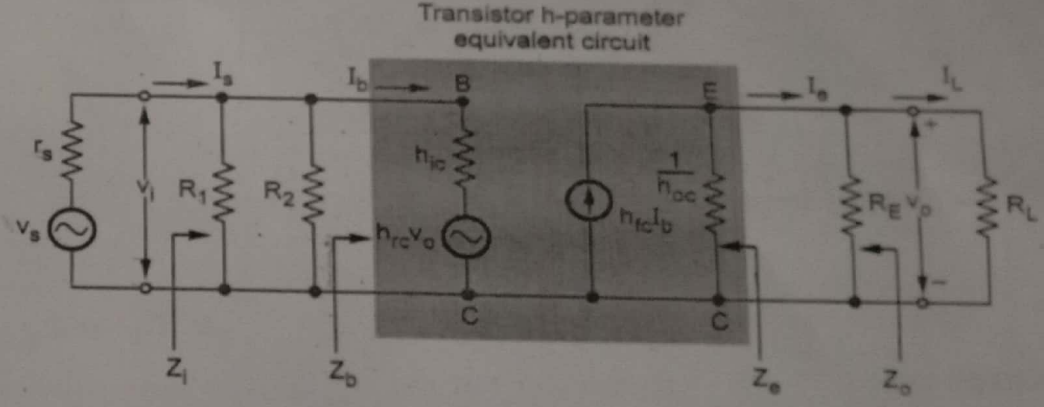


Fig. Q.25.1 (b) h - parameter equivalent circuit for CC amplifier

Input impedance (Z_b)

From Fig. Q.25.1 (b), we have

$$v_i = I_b h_{ic} + h_{rc} v_o$$

$$= I_b h_{ic} + v_o \qquad \text{Since } h_{rc} \approx 1$$

$$= I_b h_{ic} + I_e (R_E \| R_L)$$

$$= I_b (h_{ic} + h_{fc} (R_E \| R_L)) \qquad \because \frac{J_e}{I_b} = h_{fc}$$

$$\therefore \quad Z_b = \frac{v_i}{I_b} = h_{ic} + h_{fc} (R_E \| R_L)$$

Overall input impedance $(Z_i) = Z_b \| R_1 \| R_2$

Output impedance :

To determine the output impedance (Z_e) at the emitter terminal, the signal voltage is assumed to be zero and v_o is used to calculate I_e. With $v_s = 0$, I_b is given by,

$$I_b = \frac{h_{rc} v_o}{h_{ic} + (R_1 \| R_2 \| r_s)}$$

$$= \frac{v_o}{h_{ic} + (R_1 \| R_2 \| r_s)} \qquad \because h_{rc} = 1$$

and

$$I_e = h_{fc} I_b = \frac{h_{fc} v_o}{h_{ic} + (R_1 \| R_2 \| r_s)}$$

$$\therefore \quad Z_e = \frac{v_o}{I_e} = \frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}$$

Overall output impedance

$$(Z_o) = Z_e \| R_E$$

$$\approx Z_e \qquad \because R_E >> Z_e$$

Voltage gain :

From Fig. Q.25.1 (b) we have,

$$v_i = I_b [h_{ic} + h_{rc} v_o]$$

$$= I_b [h_{ic} + h_{rc} (h_{fc} I_b (R_E \| R_L))]$$

$$= I_b [h_{ic} + h_{rc} h_{fc} (R_E \| R_L)]$$

$$= I_b [h_{ic} + h_{fc} (R_E \| R_L)] \qquad \because h_{rc} \approx 1$$

and

$$v_o = I_e (R_E \| R_L)$$

$$\therefore \quad A_v = \frac{v_o}{v_i} = \frac{I_e (R_E \| R_L)}{I_b [h_{ic} + h_{fc} (R_E \| R_L)]}$$

$$= \frac{h_{fc} (R_E \| R_L)}{h_{ic} + h_{fc} (R_E \| R_L)}$$

$$= \frac{(R_E \| R_L)}{\frac{h_{ic}}{h_{fc}} + (R_E \| R_L)}$$

$$= \frac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} \qquad \because \frac{h_{ic}}{h_{fc}} = \frac{h_{ie}}{1 + h_{fe}} = h_{ib}$$

Usually, $R_E \| R_L$ is so much larger than h_{ib},

$$\therefore \quad A_v \approx 1$$

Q.26 For the circuit shown in Fig. Q.26.1, calculate Z_i and A_v with R_L not connected and with R_L connected. Assume h_{ie} = 2.1 K and h_{fe} = 100.

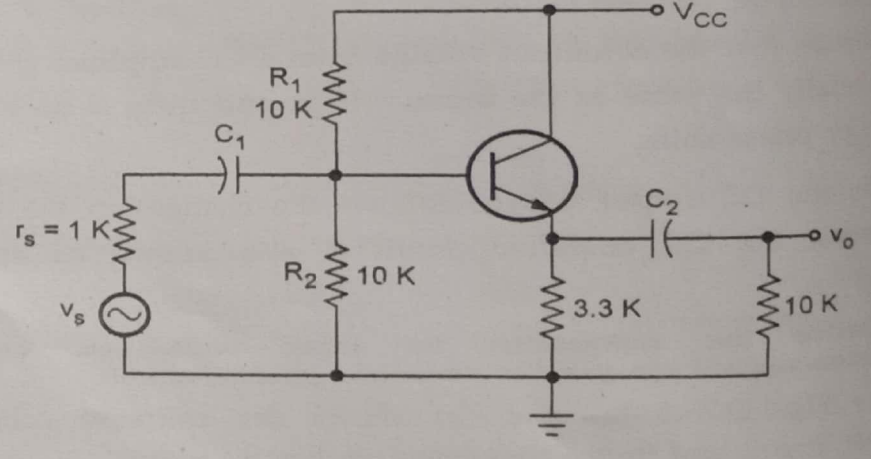


Fig. Q.26.1

: a) Without R_L :

$$h_{ic} = h_{ie} = 2.1\ k\Omega$$

$$h_{fc} = 1 + h_{fe} = 1 + 100 = 101$$

$$Z_b = h_{ic} + h_{fc}(R_E \,||\, R_L) = 2.1\ k\Omega + 101\ (3.3\ K)$$

$$= 335.4\ k\Omega$$

$$Z_i = R_1 \,||\, R_2 \,||\, Z_b = 10\ K \,||\, 10\ K \,||\, 335.4$$

$$= 4.93\ k\Omega$$

$$Z_e = \frac{h_{ic} + (R_1 \,||\, R_2 \,||\, r_S)}{h_{fc}}$$

$$= \frac{2.1K + (10K \,||\, 10K \,||\, 1K)}{101} = 29.04\ \Omega$$

$$Z_o = Z_e \,||\, R_E = 29.04 \,||\, 3.3K$$

$$= 28.79\ \Omega$$

ith R_L connected :

$$Z_b = h_{ic} + h_{fc}(R_E \,||\, R_L)$$

$$= 2.1\ k\Omega + 101\ (33K \,||\, 10K)$$

$$= 252.7\ k\Omega$$

$$Z_i = R_1 \,||\, R_2 \,||\, Z_b = 10\ K \,||\, 10\ K \,||\, 252.7\ K$$

$$= 4.9\ k\Omega$$

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}} = \frac{2.1\ k\Omega}{1 + 100} = 20.79\ \Omega$$

$$A_v = \frac{R_E \,||\, R_L}{h_{ib} + (R_E \,||\, R_L)}$$

$$= \frac{(3.3K \,||\, 10K)}{20.79 + (3.3K \,||\, 10K)}$$

$$= 0.9917$$

4.7 : Comparison of CE, CB and CC Circuits

Q.27 Give the comparison between CE, CB and CC circuits.

Ans. :

Sr. No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Low
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

END...

5 Field Effect Transistors (FET) and its Biasing

5.1 : Introduction

Q.1 What is FET ?

Ans. : • The Field Effect Transistor abbreviated as **FET** is an another semiconductor device like a BJT which can be used as an amplifier or switch.

- Like BJT, FET is also a three terminal device;
- The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. Q.1.1. Out of these three terminals gate terminal acts as a controlling terminal.

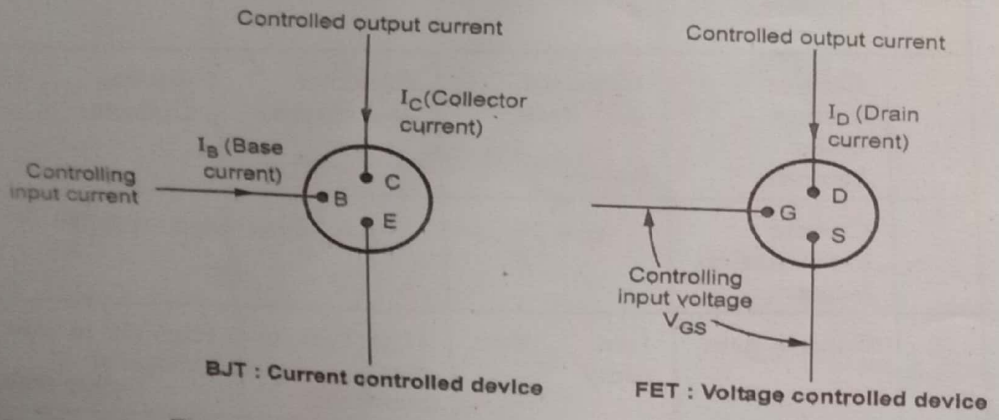


Fig. Q.1.1 Controlling element for BJT and FET

Q.2 List Important features of FET.

Ans. : Voltage Controlled Device

• Unipolar Device

- FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called **unipolar device.**
- Unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.
- FET has **very high input impedance.**
- FETs **require less space** than that for BJTs, hence they are preferred in integrated circuits.

Q.3 State the types of FET.

Ans. : • The FETs are categorised as :

- Junction Field Effect Transistors (JFETs),
- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

Q.4 Explain with neat sketch construction of n-channel FET.

OR Draw symbols of n-channel JFET.

Ans. : • The Fig. Q.4.1 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET.

- Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**
- The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. Q.4.1.

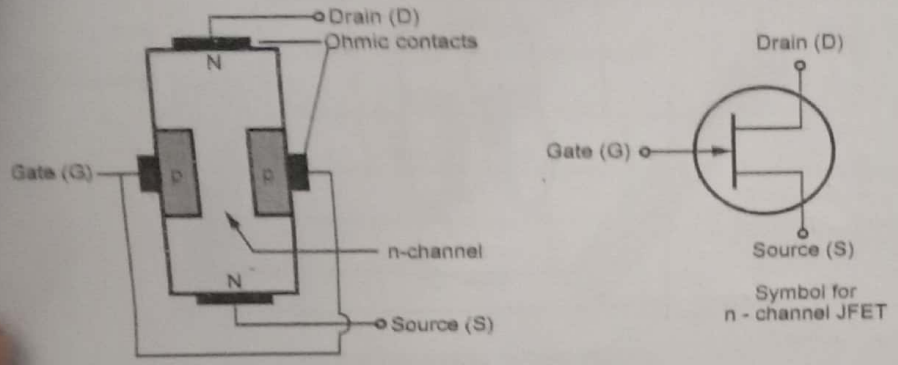


Fig. Q.4.1 Structure and symbol for n-channel JFET

Q.5 Explain with neat sketch construction of p-channel FET.

OR Draw the symbol of n-channel and p-channel JFET.

Ans. : • The device could be made of p type bar with two n type gates as shown in the Fig. Q.5.1. Then this will be **p-channel JFET.**

• The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in **n-channel JFET** the current is carried by electrons while in **p-channel JFET**, it is carried by holes.

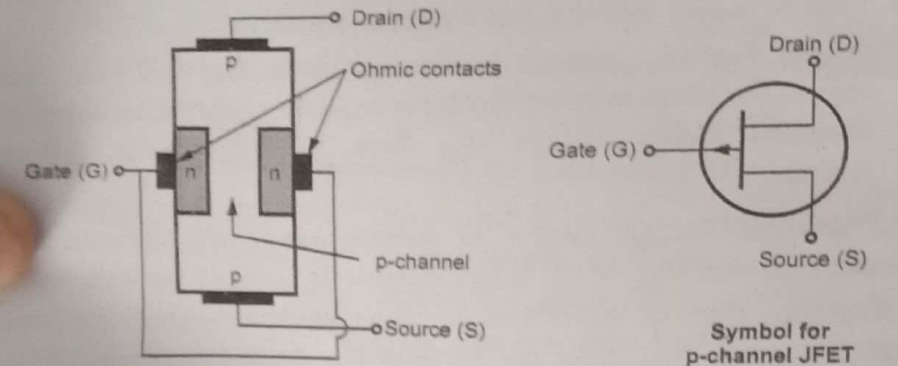


Fig. Q.5.1 Structure and symbol for p-channel JFET

Q.6 Explain the working of n-channel FET.

Ans. : • When voltage is applied between the drain and source with DC supply V_{DS}, electrons flow from source to drain through the narrow channel existing between the depletion regions. This causes a drain current ID to flow from drain to source.

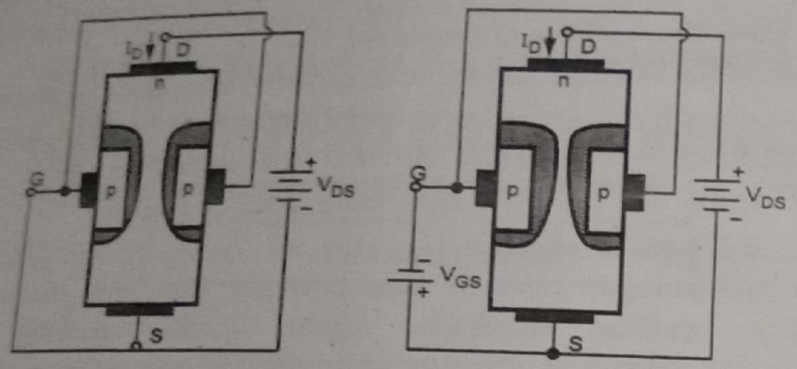
• When the gate is shorted to source as shown in Fig. Q.6.1 (a), there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS}.

• When the gate to source voltage V_{GS} is increased with negative value as shown in Fig Q.6.1 (b), the reverse bias voltage across gate to source increases. As a result, the width of the depletion region increases. This reduces the width of the channel and thus controls the drain current I_D.

• It is observed that the channel is narrower at the drain end. This happens because amount of reverse bias is not same throughout the length of p-n junction.

• When negative value of V_{GS} is increased further, a stage is reached at which two depletion regions touch each other leaving zero width for conducting portion of the channel as shown in the Fig. Q.6.1 (c). This will prevent any current flow from drain to source and hence cut off the drain current. The gate to source voltage that produces cut-off is known as **cut-off voltage** and it is denoted by $V_{GS\,(off)}$.

• From above discussion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called **voltage controlled current source.**



(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

Fig. Q.6.1 The effect of gate voltage on channel- width and on drain current I_D

Q.7 Explain the working of p-channel FET.

Ans. : • The p-channel JFET is constructed in exactly the same manner as the n-channel JFET but with reversal of the p-and n-type materials as shown in the Fig. Q.7.1.

• All current directions and voltage polarities are reversed

For V_{GS} = 0, channel width is maximum. By increasing positive gate to source (V_{GS}) voltage, the channel width is reduced.

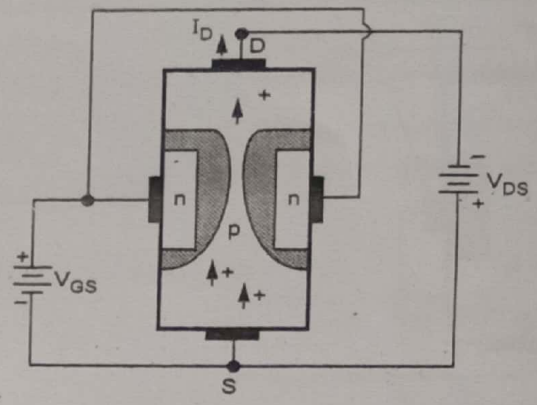


Fig. Q.7.1 p-channel FET

5.2 : JFET Characteristics

Q.8 List the important characteristics of JFET.

Ans. : The important characteristics of JFET are :

1. Drain characteristics and
2. Transfer characteristics

Q.9 Explain the drain characteristics for an n-channel FET.

OR Define pinch off voltage.

Ans. : • Fig. Q.9.1 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current and drain to source voltage for different values of V_{GS}.

1. **Ohmic Region :** Shown by curve OA in Fig. Q.9.1. In this region the drain current increases linearly with the increase in drain to source voltage V_{DS}. here, JFET acts as a simple resistor.

2. **Pinch-Off Voltage (V_p) :** At some value of V_{DS} (shown by point A for V_{GS} = 0), drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is

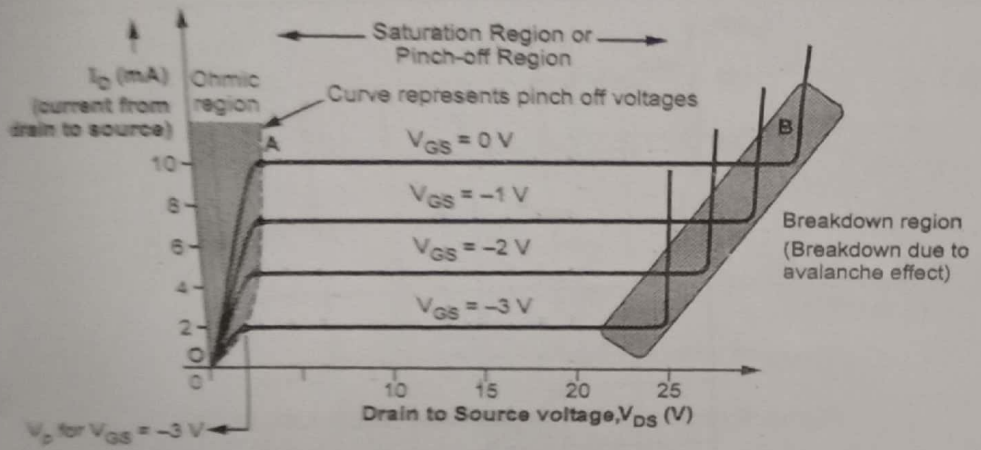


Fig. Q.9.1 Drain V-I characteristics of n-channel JFET

called **'Pinch-Off Voltage'**, V_p. From Fig. Q.9.1 it can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.

3. **Saturation Region (Pinch-off Region) :** This region shown by AB curve. In the saturation region, the drain current I_D remains fairly constant and does not vary with V_{DS}.

4. **Break down Region :** In this region the drain current increases rapidly as the drain to source voltage increases. This happens because of break down of gate to source junction due to avalanche breakdown. The drain to source voltage corresponding to point B is called breakdown voltage VBR.

5. ***Relation of $V_{GS\,(off)}$ and V_p :*** I_D is 0 when $V_{GS} = -V_P$.

Q.10 Explain the drain characteristics for p-channel FET.

Ans. : • In a p-channel JFET the source is positive with respect to the drain. Here the source is the source of holes which flow through the channel to the drain. The pinch-off is achieved by making the source to gate voltage, V_{SG} negative (i.e. V_{GS} positive) here by reverse biasing the p-n junction diode formed by the channel and the gate.

- The Fig. Q.10.1 shows the drain characteristics of p-channel JFET. Note the similarities between these characteristics and those shown for n-channel JFET in Fig. Q.9.1.

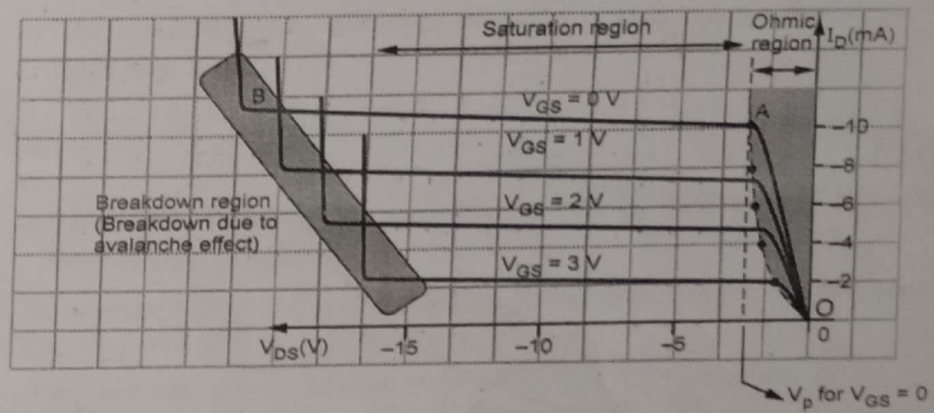


Fig. Q.10.1 Drain V-I characteristics of p-channel JFET

- The curves are identical except that voltage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

Q.11 Explain the transfer characteristics for n-channel JFET.

Ans. : Square Law Expression for I_D

- The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear as shown in the Fig. Q.11.1 This relationship is defined by **Shockley's** equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \qquad \ldots (Q.11.1)$$

- The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

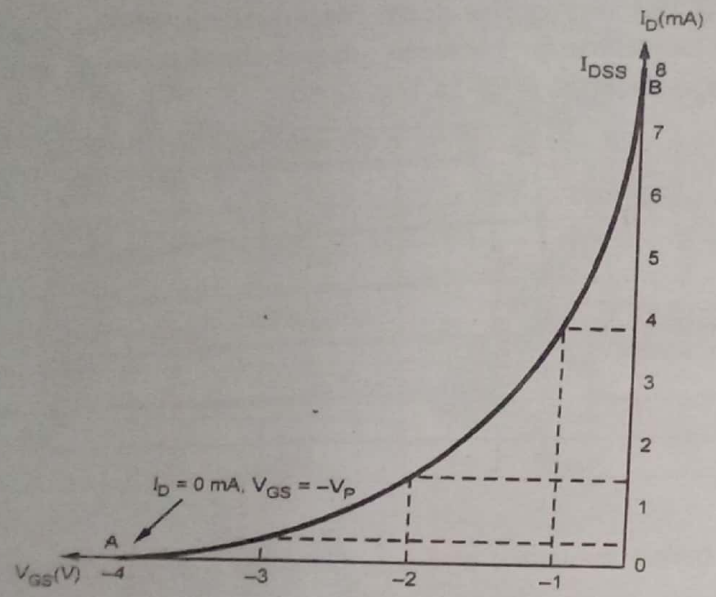


Fig. Q.11.1 Transfer characteristics of n-channel JFET

- In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D.
- A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS\,(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at V_{GS} =0). Thus, this curve shows the operating limits of a JFET. These are :
  - $I_D = 0$ when $V_{GS} = V_{GS\,(off)}$
  - $I_D = I_{DSS}$ when $V_{GS} = 0$

Q.12 Explain the transfer characteristics for p-channel JFET.

Ans. : • The Fig. Q.12.1 shows the transfer characteristics of p-channel JFET. It is identical to transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

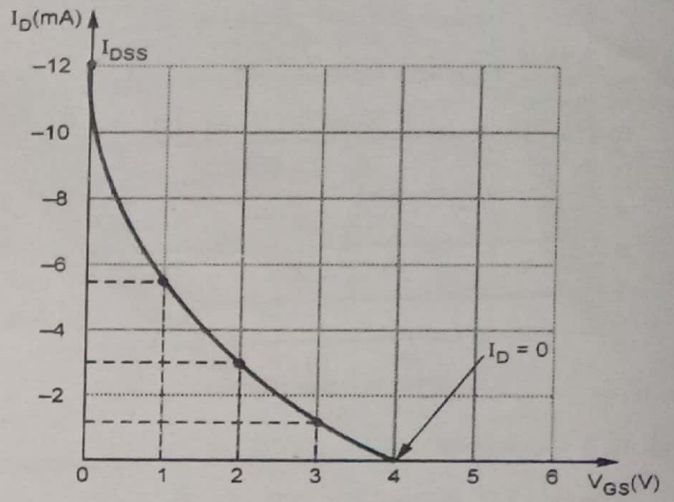


Fig. Q.12.1 Transfer characteristics of p-channel JFET

Q.13 For JFET, determine I_D, if I_{DSS} = 12 mA, V_P = – 4 V and V_{GS} = – 1.

Ans. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 12\times10^{-3}\left(1-\frac{(-1)}{(-4)}\right)^2$$

$$= 6.75 \text{ mA}$$

5.3 : FET Biasing in Ohmic Region and Active Region

Q.14 Comment on FET biasing in ohanic region and active region

Ans. : • The JFET can be biased in the ohmic or in the active region.

- When biased in the ohmic region, the JFET in equivalent to a resistance.
- When biased in the active region, the JFET is equivalent to a current source.

Q.15 Explain the gate bias circuit used to bias FET in ohmic region.

Ans. : • Fig. Q.15.1 shows the gate bias circuit for the n-channel JFET. This is the simplest biasing arrangement.

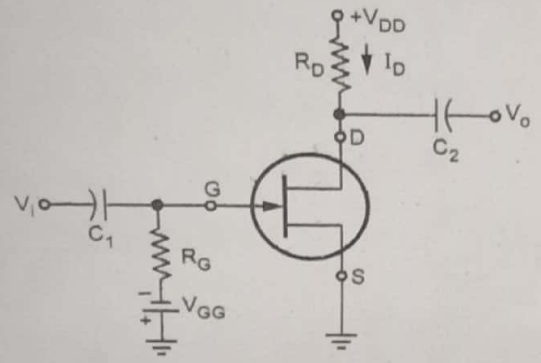


Fig. Q.15.1 Gate bias circuit for n-channel circuit

- To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.
- For the d.c. analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero.
- This permits R_G to replace by short circuit equivalent, simplifying the gate bias circuit as shown in the Fig. Q.15.2

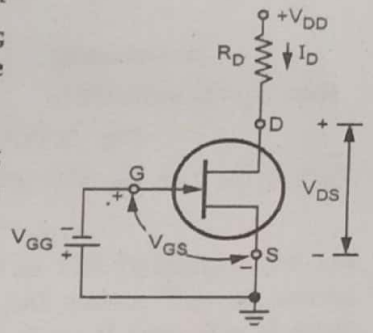


Fig. Q.15.2 Simplified gate bias circuit

Step 1 : Calculate V_{GS}

- We know for d.c. analysis $I_G = 0$ A and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$V_{GS} = -V_{GG} \qquad \ldots (Q.15.1)$$

- Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude and hence the name gate bias circuit.

Step 2 : Calculate I_{DQ}

- The drain current I_D can be calculated using equation.

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Step 3 : Calculate V_{DS}

- The drain to source voltage of drain circuit can be determined by applying KVL.

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$\therefore \quad V_{DSQ} = V_{DD} - I_D R_D \qquad \ldots (Q.15.2)$$

- The main drawback of gate bias circuit of FET is that it requires two power supplies.

To ensure that a JFET is biased in the ohmic region, all we have to use $V_{GS} = 0$ and $I_{D\,(sat)} << I_{DSS}$.

Q.16 For the circuit shown in the Fig. Q.16.1 Calculate :
a) V_{GSQ}, b) I_{DQ}, c) V_{DSQ}, d) V_D

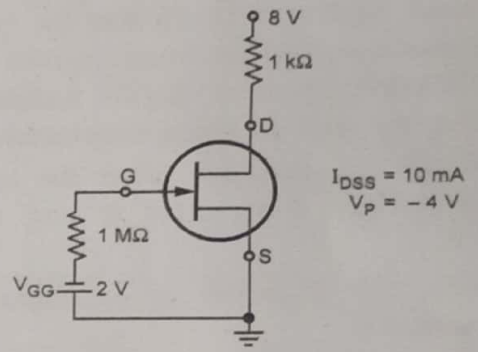


Fig. Q.16.1

Ans. :

a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$ $\quad \because I_G = 0$ and $I_G R_G = 0$

b) $$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10\times10^{-3}\left(1 - \frac{-2\ V}{-4\ V}\right)^2$$

$$= 10\times10^{-3}\,(1-0.5)^2 = 10\times10^{-3}\,(0.25) = \mathbf{2.5\ mA}$$

c) $V_{DSQ} = V_{DD} - I_{DQ} R_D = 8\ V - 2.5\times10^{-3}\,(1\times10^3) = \mathbf{5.5\ V}$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = \mathbf{5.5\ V}$

Q.17 Calculate the drain voltage for gate bias circuit with R_D = 10 kΩ. Assume that the JFET is based in the ohmic region. Assume I_{DSS} = 10 mA, V_p = 4 V and V_{DD} = 10 V.

Ans. : In the ohmic region, we can replace JFET by a resistance R_{DS}, as shown in the Fig. Q.17.1.

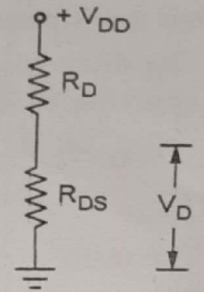


Fig. Q.17.1 JFET equivalent circuit when biased in the ohmic

$$R_{DS} = \frac{V_p}{I_{DSS}} = \frac{4}{10\text{ mA}} = 400\ \Omega$$

$$V_D = \frac{R_{DS}}{R_{DS} + R_D} V_{DD}$$

$$= \frac{400}{400 + 10\text{K}} \times 10 = \mathbf{0.385\ V}$$

Q.18 Draw and explain the self bias circuit for biasing FET in active region.

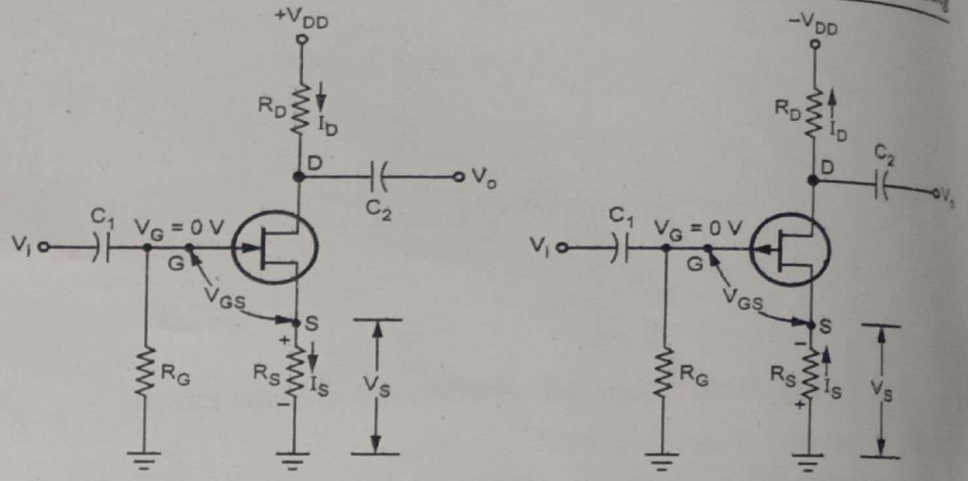
Ans. : • *JFET* must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. Q.18.1.

- The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.
- The voltage drop across resistor, R_S makes gate source junction reverse biased.

DC Analysis :

Step 1 : Obtain expression for V_{GS}

For the n-channel FET in Fig. Q.18.1 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then



(a) n-channel (b) p-channel

Note : $I_S = I_D$ in all JFETs

Fig. Q.18.1 Self bias circuits for JFET

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

For the p-channel FET in Fig. Q.18.1 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = - I_S R_S = - I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (- I_D R_S) = + I_D R_S$$

In the following D.C. analysis, the n-channel JFET shown in Fig. Q.18.1 (a) is used to for illustration. For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. Q.18.2.

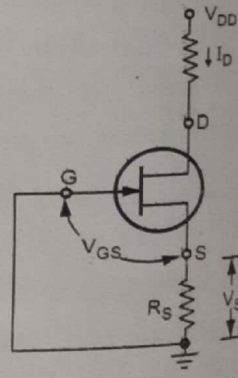


Fig. Q.18.2 Simplified self bias circuit for dc

Step 2 : Calculate I_{DQ}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \ldots (Q.18.1)$$

Step 3 : Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D = V_{DD} - I_D (R_S + R_D)$$

Q.19 For the circuit shown in Fig. Q.19.1. Calculate V_{GSQ}, I_{DQ}, V_{DS}, V_S and V_D.

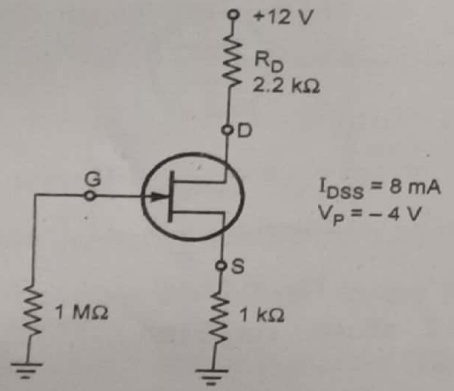


Fig. Q.19.1

Ans. : *Step 1 : Obtain expression for* V_{GS}

$$V_{GS} = -I_D R_S$$

Step 2 : Calculate I_D and Values of V_{GS} and V_S.

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2$$

$$\therefore I_D = 8\times10^{-3}\left(1 + \frac{I_D \times 1\times10^3}{-4}\right)^2 = 8\times10^{-3}\,(1 - 250 I_D)^2$$

$$= 8\times10^{-3}\,(1 - 500 I_D + 62500 I_D^2)$$

$$I_D = 8\times10^{-3} - 4 I_D + 500 I_D^2$$

$$\therefore \quad 500 I_D^2 - 5 I_D + 8\times10^{-3} = 0$$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we have,

$$= \frac{+5 \pm \sqrt{(-5^2) - 4(500)(8\times10^{-3})}}{2\times(500)}$$

$$= \frac{+5 \pm \sqrt{25 - 16}}{1000} = \frac{+5 \pm \sqrt{9}}{1000} = \frac{+5 \pm 3}{1000} = 8 \text{ mA or } 2 \text{ mA}$$

I_{DQ} cannot have value 8 mA because maximum value of I_D, I_{DSS} is given as 8 mA at $V_{GS} = 0$ and hence I_{DQ} is taken as **2 mA**.

$$\therefore V_{GS_Q} = -I_D R_S = -2\times10^{-3}\times1\times10^3 = \mathbf{-2\ V}$$

$$V_S = I_D R_S = 2\times10^{-3}\times1\times10^3 = \mathbf{2\ V}$$

Step 3 : Calculate V_{DS}

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - 2\times10^{-3}(2.2\times10^3 + 1\times10^3)$$

$$= 12 - 6.4 = \mathbf{5.6\ V}$$

Step 4 : Calculate V_D

$$V_D = V_{DS} + V_S = 5.6 + 2 = \mathbf{7.6\ V}$$

Q.20 Calculate the value of feedback resistor (R_s) required to self bias an n-channel JFET with I_{DSS} = 40 mA, V_P = – 10 and V_{GSQ} = – 5 V.

Ans. :

Step 1 : Calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GSQ}}{V_P}\right]^2 = 40\times10^{-3}\left[1 - \frac{(-5)}{(-10)}\right]^2 = \mathbf{10\ mA}$$

Step 2 : Calculate R_S

For self bias circuit : $V_{GSQ} = -I_{DQ} R_S$

$$R_s = \frac{-V_{GSQ}}{I_{DQ}} = \frac{-(-5)}{10\text{ mA}} = 500\ \Omega$$

Q.21 V_p = – 2 V, I_{DSS} = 1.65 mA for the circuit in Fig. Q.21.1. It is desired to bias the circuit at I_D = 0.8 mA, V_{DD} = 24 V. Calculate i) V_{GS} ii) g_m iii) R_S

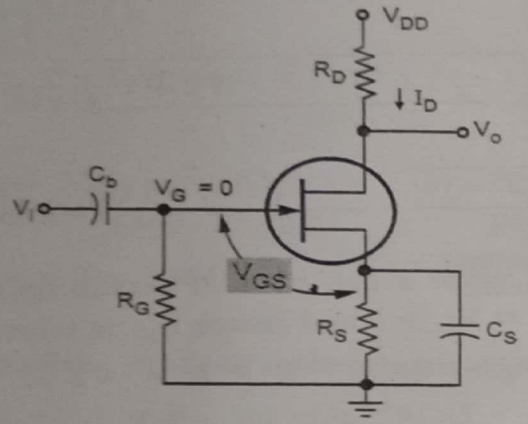


Fig. Q.21.1

Ans. : **Step 1 :** Calculate V_{GS}

We have $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$

$$\therefore \quad V_{GS} = V_p\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right) = -2\left(1-\sqrt{\frac{0.8\times10^{-3}}{1.65\times10^{-3}}}\right)$$

$$= -0.6074\ \text{V}$$

Step 2 : Calculate g_m

$$g_{mo} = \frac{-2I_{DSS}}{V_p} = \frac{-2\times1.65}{-2} = 1.65\ \text{mS}$$

$$g_m = g_{mo}\left[1-\frac{V_{GS}}{V_p}\right] = 1.65\left(1-\frac{0.6074}{2}\right)\times10^{-3}$$

$$= 1.65\times10^{-3}\times0.6963 = 1.15\ \text{mS}$$

Step 3 : Calculate R_S

$$0 = V_{GS} + I_D R_S$$

$$\therefore \quad R_S = -\frac{V_{GS}}{I_D} = -\left(\frac{0.6074}{0.8\text{ mA}}\right) = 759.25\ \Omega$$

Q.22 The FET shown in Fig. Q.22.1 has $|I_{DSS}|$ = 12 mA and $|V_p|$ = 5 V. Calculate the quiescent values of i) I_D ii) V_{DS} iii) V_{GS}.

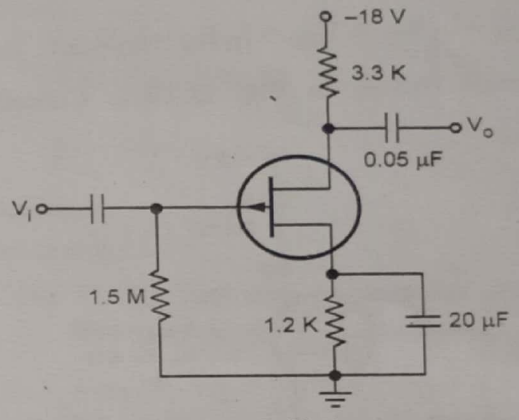


Fig. Q.22.1

Ans. : Fig. Q.22.2 shows simplified circuit for d.c. analysis

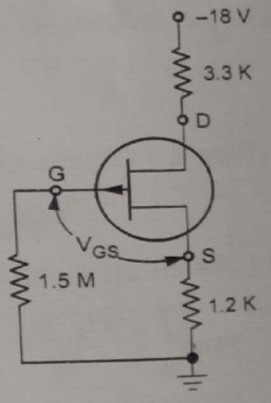


Fig. Q.22.2

Step 1 : Obtain expression for V_{GS}.

Applying KVL to the input circuit we get,

$$V_{GS} - I_D R_S = 0$$

$$\therefore \quad V_{GS} = I_D R_S$$

Step 2 : Calculate I_D

We have, $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$

Substituting value of V_{GS} in above equation and solving for I_D we get,

$$I_D = 2.33\ \text{mA or } 7.45\ \text{mA}$$

We calculate V_{DS} using $I_D = 7.45$ mA

$$V_{DS} = V_{DD} - [- I_D (R_S + R_D)]$$

$$= - 18 - [- 7.45 (1.2 \times 10^3 + 3.3 \times 10^3)]$$

$$= - 18 + 33.525 = 15.525 \text{ V}$$

Practically, value of V_{DS} for p-channel FET should be negative, hence value of $I_D = 7.45$ mA is invalid.

$\therefore$ I_D = **2.33 mA**

Step 3 : Calculate V_{DS} and V_{GS}.

Now calculating V_{DS} taking $I_D = 2.33$ mA

$$V_{DS} = V_{DD} - [- I_D (R_S + R_D)]$$

$$= - 18 - [- 2.33 \times 10^{-3} (1.2 \times 10^3 + 3.3 \times 10^3)]$$

$$= - 18 + 10.485 = \mathbf{- 7.515 \text{ V}}$$

$$V_{GS} = I_D R_S = 2.33 \times 10^{-3} \times 1.2 \times 10^3 = \mathbf{2.796 \text{ V}}$$

Q.23 Draw and explain the voltage divider bias circuit for biasing FET in active region.

Ans. : • The Fig. Q.23.1 shows n-channel JFET with voltage divider bias.

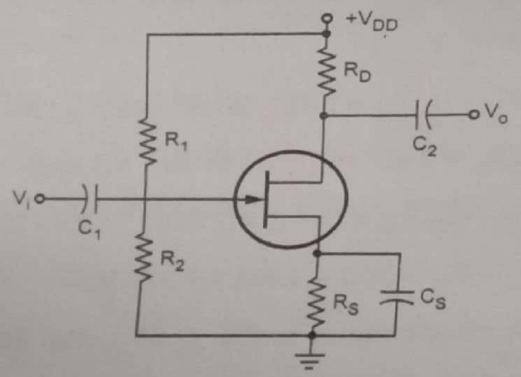


Fig. Q.23.1 Voltage divider bias for n-channel JFET

- The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.
- The source voltage is,

$$V_S = I_D R_S$$

- The gate voltage is set by resistors R_1 and R_2.
- Coupling capacitors C_1 and C_2 and source resistor bypass capacitor C_S are assumed to be open circuit for DC analysis.

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} \qquad \because I_G = 0$$

Step 2 : Obtain expression for V_{GS}

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - I_D R_S = 0$$

$$\therefore \quad V_{GS} = V_G - I_D R_S \quad \ldots \text{(Q.23.1)}$$

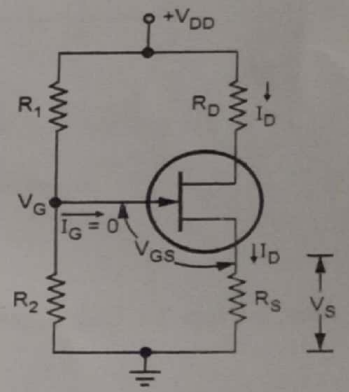


Fig. 6.5.9 Simplified voltage divider circuit for d.c. analysis

Step 3 : Calculate I_{DQ}

The I_{DQ} can be calculated using equation :

$$I_{DQ} = I_{DSS} \left[1 - \frac{V_{GS}}{V_p}\right]^2$$

Step 4 : Calculate V_{DS} and V_{GS}

Applying KVL to the output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S) \quad \ldots \text{(Q.23.2)}$$

The Q point of a JFET amplifier using the voltage divider bias is given by :

$$I_{DQ} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D\,(R_D+R_S)$$

$$V_{GSQ} = V_G - I_D R_S$$

Q.24 Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network of Fig. Q.24.1.

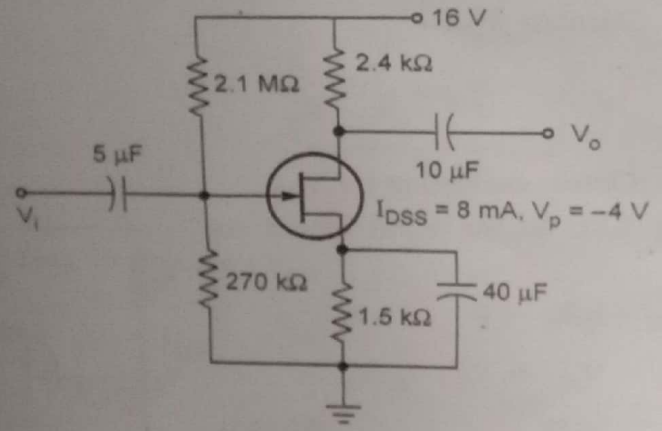


Fig. Q.24.1

Ans. : Step 1 : Calculate V_G

$$V_G = \frac{V_{DD}R_2}{R_1+R_2} = \frac{16\times 270\,K}{2.1\,M+270\,K} = 1.823\ V$$

Step 2 : Obtain expression for V_{GS}

$$\therefore \quad V_{GS} = 1.823 - I_D\,R_S = 1.823 - 1.5\times 10^3\,I_D$$

Step 3 : Calculate I_D

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 8\times 10^{-3}\left(1-\frac{(1.823-I_D\times 1.5\times 10^3)}{-4}\right)^2$$

$$= 8\times 10^{-3}\left(1-[(-0.456+375\,I_D)]\right)^2 = 8\times 10^{-3}(1.456-375\,I_D)^2$$

$$= 8\times 10^{-3}\left(2.12-1092\,I_D+140625\,I_D^2\right)$$

$$I_D = 0.01696 - 8.736\,I_D + 1125\,I_D^2$$

$$\therefore\ 1125\,I_D^2 - 9.736\,I_D + 0.01696 = 0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we get,

$$= \frac{-(-9.736)\pm\sqrt{(-9.736)^2-4\times 1125\times 0.01696}}{2\times 1125} = \frac{9.736\pm 4.2976}{2\times 1125}$$

$$= \mathbf{6.237\ mA} \quad \text{or} \quad \mathbf{2.417\ mA}$$

If we calculate value of V_{DS} taking I_D = 6.237 mA we get,

$$V_{DS} = V_{DD} - I_D(R_D+R_S) = 16 - 6.237\times 10^{-3}(2.4\,K+1.5\,K)$$

$$= \mathbf{-\ 8.3243\ V}$$

Practically, the value of V_{DS} must be positive, hence

I_D = 6.237 mA is invalid.

$$\therefore \quad I_D = \mathbf{2.417\ mA}$$

Step 4 : Calculate V_{DS}, V_{GS}, V_S, V_D and V_{DG}.

$$\therefore V_{DS} = V_{DD} - I_D(R_D+R_S) = 16 - 2.417\times 10^{-3}(2.4\,K+1.5\,K)$$

$$= \mathbf{6.5737\ V}$$

$$V_{GS} = 1.823 - I_D\,R_S = 1.823 - (2.417\times 10^{-3}\times 1.5\times 10^3) = \mathbf{-\ 1.8025\ V}$$

$$V_S = I_D R_S = 2.417\times 10^{-3}\times 1.5\times 10^3 = \mathbf{3.6255\ V}$$

$$V_D = V_{DD} - I_D R_D = 16 - (2.417\times 10^{-3}\times 2.4\times 10^3) = \mathbf{10.2\ V}$$

$$V_{DG} = V_D - V_G = 10.2 - 1.823 = \mathbf{8.377\ V}$$

Q.25 For the circuit shown in Fig. Q.25.1, the FET has V_p = 4 V, I_{DSS} = 4 mA
Calculate i) I_{DSQ} ii) V_{GSQ} iii) V_{DSQ}

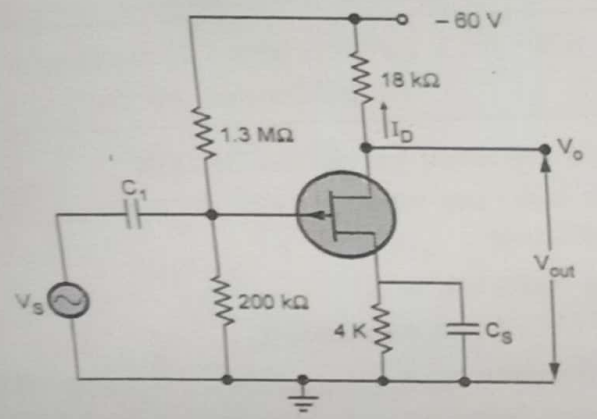


Fig. Q.25.1

Ans. : Simplified circuit for d.c. analysis is shown in Fig. Q.25.2.

Step 1 : Calculate V_G

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{200\times10^3 \times(-60)}{1.3\times10^6 + 200\times10^3} = -8 \text{ V}$$

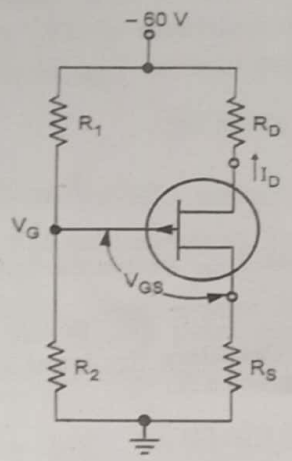


Fig. Q.25.2

Step 2 : Obtain expression for V_{GS}

Applying KVL to input circuit we get,

$$V_G - V_{GS} + I_D R_S = 0$$

$$V_{GS} = V_G + I_D R_S$$

$$V_{GS} = V_G + I_D R_S$$

$$= -8 + I_D R_S$$

Step 3 : Calculate I_D

We have, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in the above equation and solving for I_D we get,

$$I_D = 2.25 \text{ mA or } 4 \text{ mA}$$

We calculate V_{DS} using $I_D = 4$ mA,

$$V_{DS} = V_{DD} - (-I_D (R_S + R_D))$$

$$= -60 + 4\times10^{-3}(4\times10^3 + 18\times10^3) = -60 + 88 = \mathbf{28\ V}$$

Practically, value of V_{DS} for p-channel FET should be negative, hence value of $I_D = 4$ mA is invalid.

$\therefore$ $$I_D = \mathbf{2.25\ mA}$$

Step 4 : Calculate V_{DS} and V_{GS}.

Now calculating V_{DS} taking $I_D = 2.25$ mA,

$$V_{DS} = -60 - (-2.25\times10^{-3}(4\times10^3 + 18\times10^3))$$

$$= \mathbf{-60 - 49.5 = -10.5\ V}$$

$$V_{GS} = -8 + I_D R_S = -8 + 2.25\times10^{-3}(4\times10^3) = -8 + 9 = \mathbf{1\ V}$$

Q.26 For the network shown in Fig. Q.26.1, determine I_D, V_{GS}, V_G, V_D, V_S and V_{DS}.

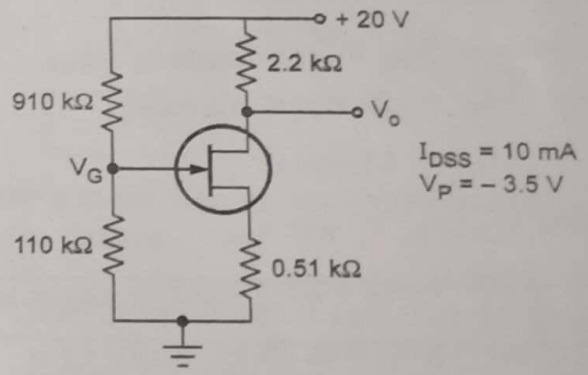


Fig. Q.26.1

Ans. :

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD}R_2}{R_1+R_2} = \frac{20 \times 110}{910 + 110} = 2.157 \text{ V}$$

Step 2 : Obtain expression of V_{GS}

$$\therefore \quad V_{GS} = V_G - V_S = 2.157 - I_D R_S = 2.157 - 510\ I_D$$

Step 3 : Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\times10^{-3}\left(1 - \frac{(2.157 - 510\ I_D)}{-3.5}\right)^2$$

Solving for I_D we get,

$$I_D = 20.98 \text{ mA or } 5.863 \text{ mA}$$

For $I_D = 20.98$ mA

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 20 - 20.98\ (2.2 + 0.51)$$

$$= -36.85 \text{ V}$$

Practically, the value of V_{DS} must be positive, hence

$I_D = 20.98$ mA is invalid.

$$\therefore \quad I_D = 5.863 \text{ mA}$$

Step 4 : Calculate V_{GS}, V_D, V_S and V_{DS}

$$V_{GS} = 2.157 - I_D R_S = 2.157 - 5.863 \times 0.51 = -0.833 \text{ V}$$

$$V_D = V_{DD} - I_D R_D = 20 - 5.863 \times 2.2 = 7.1 \text{ V}$$

$$V_S = I_D R_S = 5.863 \times 0.51 = 2.99 \text{ V}$$

$$V_{DS} = V_D - V_S = 7.1 - 2.99 = 4.11 \text{ V}$$

5.4 : JFET Parameters - Transconductance, Amplification Factor

Q.27 List the important parameters of JFET.

Ans. : • The important parametres of JFET are as follows :

- Input resistance
- DC drain resistance
- Dynamic (AC) Drain resistance (r_d)
- Transconductance (g_m)
- Amplification factor (μ)

Q.28 What is the input resistance of JFET ?

Ans. : • The input junction of JFET (gate - source junction) is reverse-biased and hence its input resistance is very high. The input resistance of JFET can be determined from a value of the gate reverse current, I_{GSS} at a certain gate-to-source voltage.

It is given by,

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

- Since I_{GSS} increases with temperature, input resistance decreases with temperature.

Q.29 Calculate the input resistance of JFET if $I_{GSS} = -2$ nA when $V_{GS} = -15$ V.

Ans. :

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{15}{2\times10^{-9}} = 7500 \text{ M}\Omega$$

Q.30 What is DC drain resistance ?

Ans. : • The DC drain resistance is the resistance between drain and source terminals for the corresponding value of drain current, I_D and V_{DS}. It is denoted by R_D and mathematically given by,

$$R_D = \frac{V_{DS}}{I_D}$$

- Its value is few hundred kΩ.

Q.31 What is AC (Dynamic) drain resistance ?

Ans. : • The drain resistance r_d is the a.c. resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain characteristic in the saturation region.

It is given by,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\text{ constant}}$$

Q.32 What is JFET forward transconductance ?

Ans. : • The forward transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant.

The forward transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\text{ constant}}$$

It is the slope of the transfer characteristic.

The forward transconductance g_m is also called **mutual conductance**. The practical unit for g_m is mS (millisiemen) or mA/V.

We can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \quad \ldots (Q.32.1)$$

where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by,

$$g_{mo} = \frac{-2 I_{DSS}}{V_p} \quad \ldots (Q.32.2)$$

This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \quad \ldots (Q.32.3)$$

• Differentiating this equation with respect to V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2 I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] \quad \text{where} \quad g_{mo} = \frac{-2 I_{DSS}}{V_p}$$

Q.33 For JFET, if I_{DSS} = 20 mA, $V_{GS(off)}$ = – 5 V, and g_{mo} = 4 mS or mA/V. Determine the transconductance for V_{GS} = – 4 V, and find I_D at this point.

Ans. : From equation (Q.32.1) we have,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] = 4\times10^{-3}\left[1 - \frac{-4\text{ V}}{-5\text{ V}}\right]$$

$$= 4\times10^{-3}\times 0.2 = 0.8\text{ mS}$$

We have, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 20\times10^{-3}\left[1 - \frac{-4\text{ V}}{-5\text{ V}}\right]^2$

$$= 20\times10^{-3}\times 0.04 = \mathbf{0.8\text{ mA}}$$

Q.34 What is amplification factor of JFET ?

Ans. : • The amplification factor, denoted by μ is defined as,

Amplification factor, $\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D\text{ constant}}$

$$\therefore \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}\times\frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \boxed{\mu = r_d \times g_m}$$

Since the parameter μ is the ratio of two similar quantities viz. ratio of two voltages; μ is unitless.

5.5 : JFET Amplification and Switching

Q.35 Explain the operation of JFET as a switch

Ans. : • For n-channel JFET when V_{GS} is sufficiently negative, I_D is reduced to 0. This represents OFF condition of switch. At this

condition (cut-off) the value of V_{GS} is designated as V_{GS} (off). The ON resistance of JFET range from about 100 Ω to 100 K. When JFET is heavily driven i.e. when V_{GS} is more positive in case of n-channel JFET $r_{d\ (ON)}$ is minimum (about 100 Ω). This represents ON condition of switch. The bipolar transistor has the advantage over the field effect device in that ON-resistance is usually only a few ohms, and hence is much smaller than ON-resistance of JFET.

- In short, we can say that by making $V_{GS} = V_{GS}$(off) we can open the switch and by making V_{GS} sufficiently positive we can close the switch.

- Fig. Q.35.1 shows JFET as an analog switch V_{GS} is either 0 V, which causes the JFET to conduct, or V_G, a negative voltage that cuts the JFET off. The output voltage of the switch, v_o is the drain to source voltage, which will be either v_d (when JFET is cut-off) or close to 0 (when the JFET is conducting).

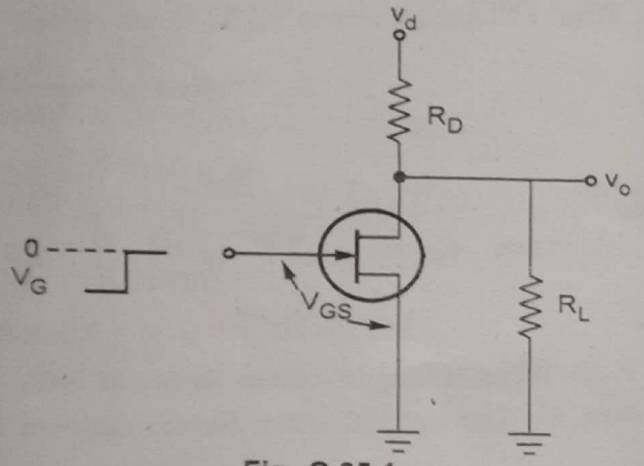


Fig. Q.35.1

Q.36 Write a note on JFET as an amplifier.

Ans. : • Let us discuss the use of the JFET as an amplifier by considering the common-source circuit, shown in the Fig. Q.36.1.

- The voltage V_{GG} provides the necessary reverse-bias between gate and source of the JFET. The signal to

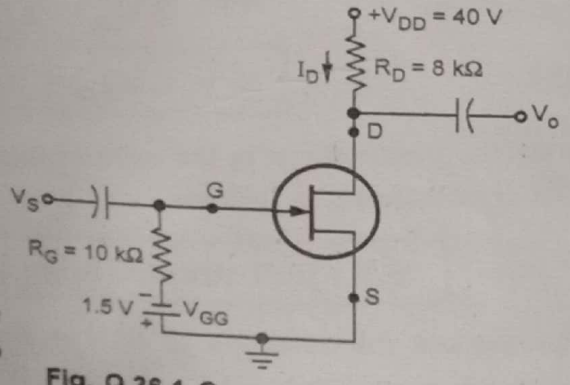


Fig. Q.36.1 Common source circuit

be amplified is V_s. The V-I characteristics of the JFET is as shown in Fig. Q.36.1.

- On the output characteristics, a load line corresponding to V_{DD} = 40 V and R_D = 8 kΩ is constructed. The transistor is biased at point Q and results in V_{DSQ} = 20 V and I_{DQ} = 2.70 mA.

- Assuming that the signal voltage V_s is a sinusoid of peak voltage V_m = 0.5 V, this signal is superimposed on the quiescent level. The instantaneous gate-to source voltage is

$$V_{gs} = V_s - V_{GG}$$

- Both quantities, I_D and V_{DS}, can be considered as sinusoids superimposed on the d.c. values.

Then
$$V_{GS} = -V_{GG} + V_{gs} = -1.5 + 0.5 \sin \omega t$$

$$I_D = I_{DQ} + i_d = 2.70 + 0.5 \sin \omega t \text{ mA}$$

$$V_{out} = V_{DS} = V_{DSQ} + v_{ds} = 20 + 4 \sin \omega t$$

- We observe that the output signal is greater than the input signal, thus indicating amplification.

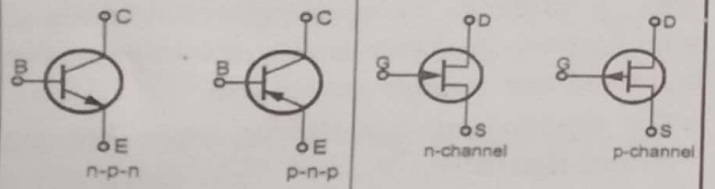
- The magnitude of the voltage gain $|A_v|$ is the ratio of the output a.c. signal amplitude [4.0 V] to the input a.c. signal amplitude [0.5 V]. Then, in this example,

$$|A_v| = \frac{4.0}{0.5} = 8$$

5.6 : Comparison of BJT and JFET

Q.37 Give comparison between BJT and FET.

Ans. :

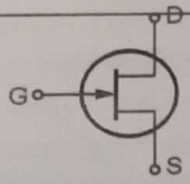
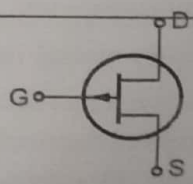
Sr. No.	Parameter	BJT	FET
1.	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2.	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3.	Types	n-p-n and p-n-p	n-channel and p-channel.
4.	Symbols		
5.	Configurations	CE, CB, CC	CS, CG, CD
6.	Input resistance	Less compare to JFET.	High compare to BJT.
7.	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in Integrated - Circuits (IC).
8.	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9.	Thermal stability	Less	More

10.	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11.	Relation between input and output	Linear	Non-linear
12.	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13.	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14.	Gain bandwidth product	High	Low

5.7 : Comparison of N-channel and P-channel JFET

Q.38 Give comparison between N-channel and P-channel JFET.

Ans. :

Sr. No.	N-channel JFET	P-channel JFET
1.	Symbol 	Symbol 
2.	Electrons are the current carriers.	Holes are the current carriers.

3.	Mobility of electrons is large in N-channel JFET.	Mobility of holes is poor in P-channel JFET.
4.	Input noise is less.	Input noise is more.
5.	Large transconductance.	Less transconductance.

5.8 : JFET Advantages, Disadvantages and Applications

Q.39 List the advantages of JFET.

Ans. : The advantages of FET are :

1. Extremely high input impedance, typically, of 100 meg-ohms.
2. Lower noise than BJT.
3. Easier to fabricate and are particularly suitable for ICs.
4. No offset voltage such as base-to-emitter voltage in BJT. This property is very important in the applications like switch, chopper, etc.
5. Immune to radiation.
6. Better thermal stability.
7. Low input capacitance.
8. Low frequency drift.
9. Draws very low power in the digital circuitry.

Q.40 List the disadvantages of JFET.

Ans. : Disadvantages of FET are :

1. Poor performance at high frequency.
2. Small gain-bandwidth in comparison to the BJT.
3. Poor voltage gain.
4. Can be operated only in low power applications.

Q.41 List the applications of JFET.

Ans. : Applications of FET are :

- In general, like BJTs the FETs can be used in switch, digital and linear amplifier applications. Let us see specific applications of FET.

- Since JFET has high input impedance and low output impedance they are used as a buffer in measuring instruments.
- Because of low noise, they are used in RF amplifiers in FM tuners and in communication equipments.
- Since the input capacitance of FET is low, it is used in cascade amplifiers in measuring and test equipments.
- FETs are used in mixer circuits in FM and TV receivers, and communication equipments. Since use of FET reduces inter modulation distortion.
- Because of low frequency drift they are used in oscillators.
- FETs are also used in low frequency amplifiers.
- FETs are used in digital circuits.

Q.42 Explain JFET as multiplexer.

Ans. : • Multiplex means many into one. Fig. Q.42.1 shows JFET as a multiplexer. It allows analog information from several sources to be routed into a single output line.

- The selection of a particular input line is controlled by gate control signals (V_1, V_2 and V_3).
- When gate control signal is high, its input signal is transmitted to the output.

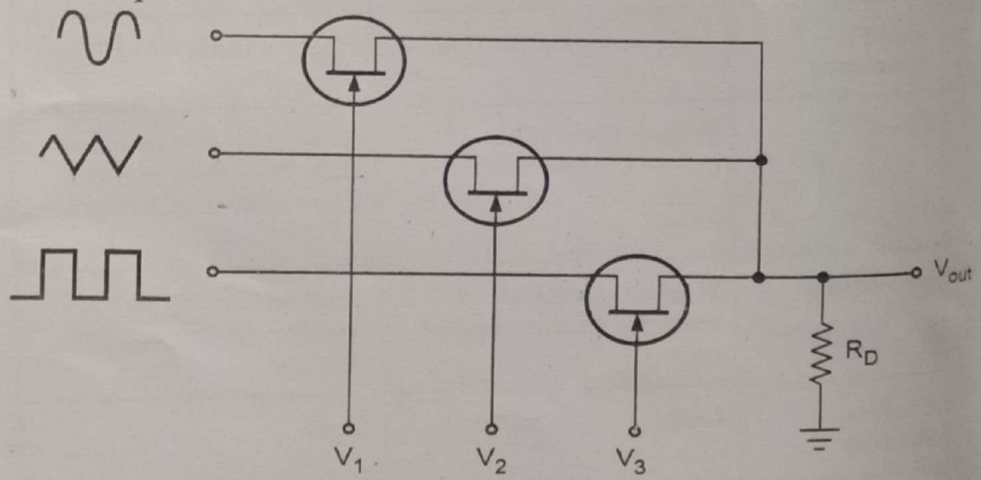


Fig. Q.42.1 Analog multiplexer

nally, only one of control signals is high; this ensures that only one of the input signals is transmitted to the output.

43 Explain the use of JFET in chopper amplifier.

ns. : • We can coupled direct coupled amplifier by connecting the tput of each stage directly to the input of the next stage.

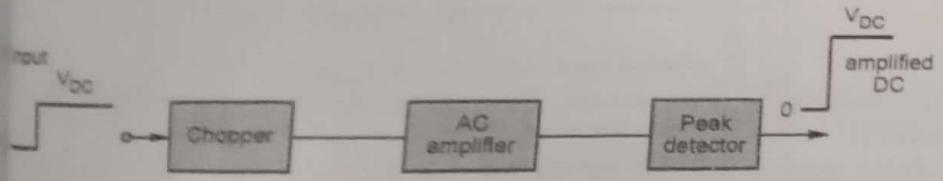
Direct coupled amplifiers couple the dc voltages and amplify them. Thus they are also called **dc amplifiers.**

The major disadvantage of direct coupling is drift, a slow shift in the final dc output voltage produced by minor changes in the supply voltage, transistor parameters and temperature variations.

One way to solve this drift problem of direct coupling is to use FET chopper.

Using JFET chopper we can control DC signal into ac square wave signal. This ac square wave signal can be amplified using conventional ac amplifier, one with coupling and bypass capacitors.

The amplified ac square wave output can then be peak detected to recover an amplified dc signal.



(a) Chopper amplifier

(b) Chopped low frequency signal

Fig. Q.43.1

- The chopper amplifier can amplify low frequency as well as dc signals.
- Fig. Q.43.1 (b) shows the chopped low frequency signal. This signal can be amplified using chopper amplifier. The amplified signal can then peak-detected to recover the original input signal.

5.9 : MOSFET

Q.44 What is MOSFET ? State its types.

Ans. : • MOSFET (Metal Oxide Semiconductor Field Effect Transistor). It is a second category of field effect transistor.

- The MOSFETs, compared to BJTs, can be made very small and hence can be used to design high density VLSI circuits.
- The MOSFET differs from the JFET in that it has no p-n junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called **IGFETs.**

Types of MOSFET

- The two basic types of MOSFETs are :
  - Depletion (D) MOSFET and
  - Enhancement (E) MOSFET.
- The terms depletion and enhancement define their basic mode of operation.

Q.45 Explain construction of n - channel depletion type MOSFET.

Ans. : • The Fig. Q.45.1 shows the basic construction of n-channel depletion type MOSFET. Two highly doped n-regions are diffused into a lightly doped p-type substrate. These two highly doped n-regions represent source and drain.

- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig. Q.45.1.

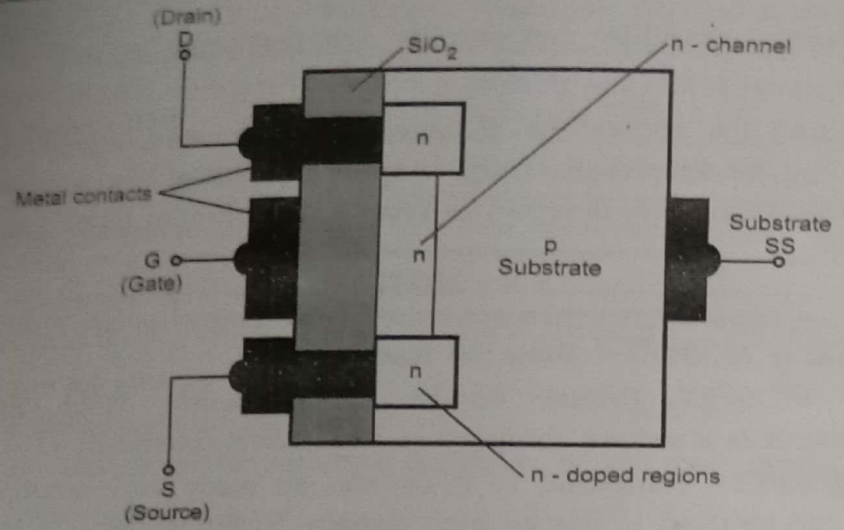


Fig. Q.45.1 n-channel depletion-type MOSFET

- The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

Q.46 Explain working of n - channel depletion type MOSFET.

Ans. : • On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V.

- On application of negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p-type substrate. This initiates recombination of repelled electrons and attracted holes.
- Due to recombinations, n-channel is depleted of free electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of

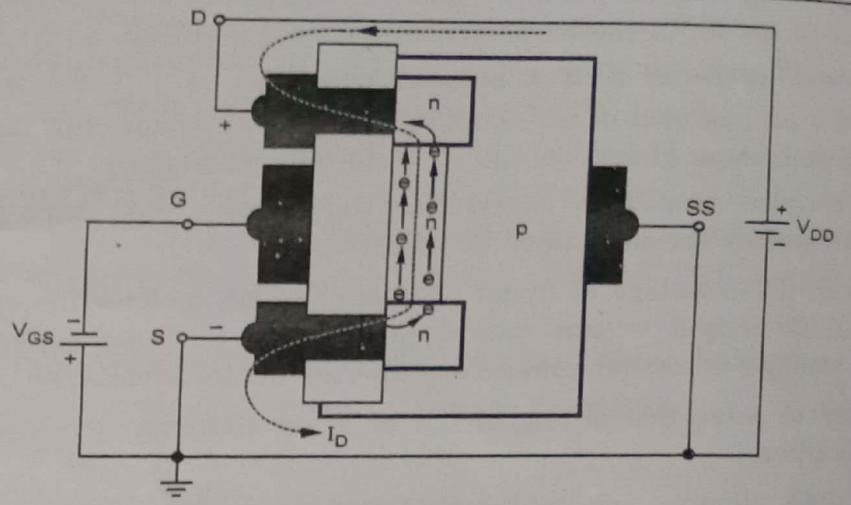


Fig. Q.46.1 n-channel depletion type MOSFET with V_{GS} = 0V and and applied voltage V_{DD}

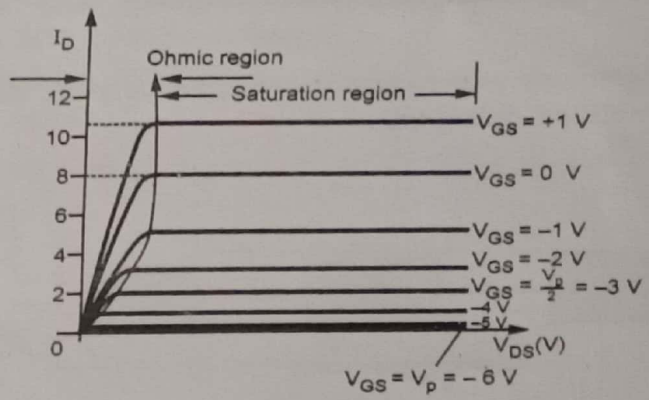


Fig. Q.46.2 Drain characteristics for an n-channel depletion type MOSFET

n-channel electrons. Thus, the level of drain current will reduce with increasing negative bias for V_{GS}.

- Fig. Q.46.2 shows drain and transfer characteristics of n - channel depletion type MOSFET.
- The square law expression for the JFET also applies to the D-MOSFET

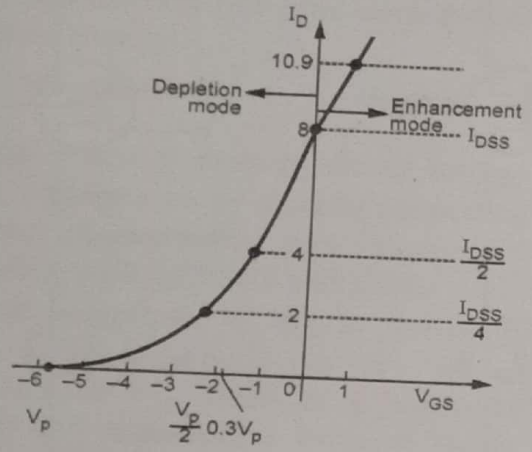


Fig. Q.46.3 Transfer characteristics for an n-channel depletion type MOSFET

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

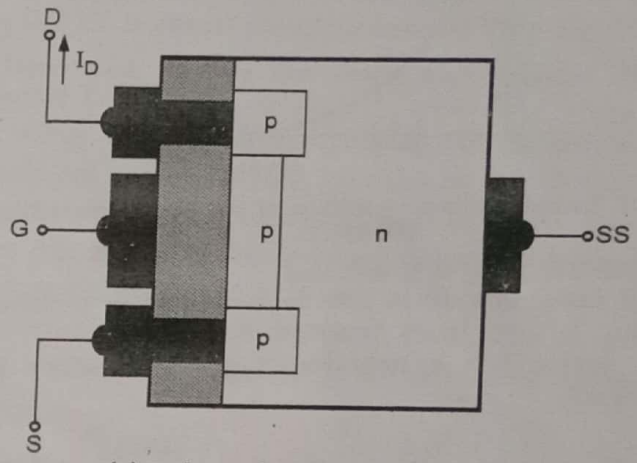
$$\approx I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Q.47 Explain the construction of p - channel depletion type MOSFET.

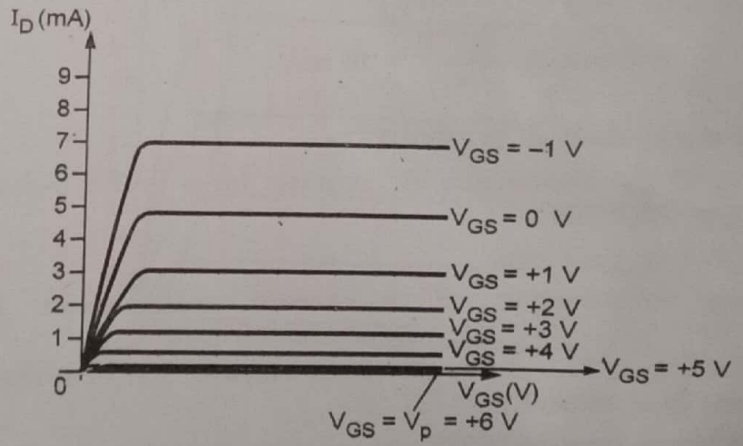
Ans. : • The construction of the p-channel depletion type MOSFET is exactly opposite of that of n-channel depletion type MOSFET. Here, the substrate is of n-type, and regions and channel are of p type as shown in the Fig. Q.47.1 (a).

• As shown in the Fig. Q.47.1 (a) voltage polarities and current directions are reversed. The drain characteristics appear exactly as in Fig. Q.47.1 (b) but V_{DS} with negative values, I_D in the opposite direction and V_{GS} having opposite polarities as shown in the Fig. Q.47.1 (b).

• Fig. Q.47.1 (c) shows the transfer characteristics of p-channel depletion type MOSFET. In the p-channel depletion type MOSFET, the transfer characteristics is a mirror image about the I_D axis (Y axis) of the transfer characteristic of n-channel depletion type MOSFET, since the V_{GS} is positive in p-channel depletion region.



(a) p-channel depletion type MOSFET



(b) Drain characteristics of p-channel depletion type MOSFET

Fig. Q.47.1

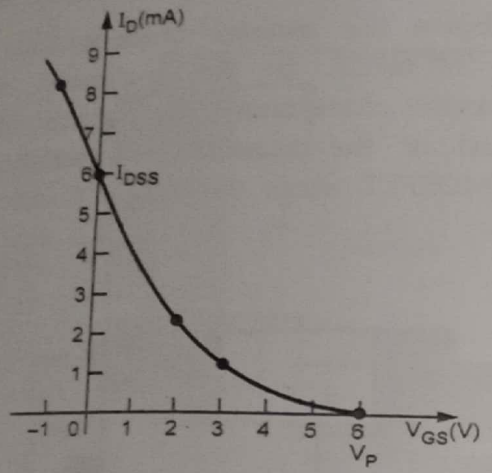


Fig. Q.47.1 (c) Transfer characteristics of p-channel depletion type MOSFET

Q.48 For D-MOSFET, I_{DSS} = 8 mA and $V_{GS(off)}$ = – 4 V determine, a) Is this an n-channel or p-channel ? b) I_D at V_{GS} = – 2 V c) I_D at V_{GS} = + 2 V

Ans. : a) The device has a negative $V_{GS(off)}$, therefore it is an n-channel MOSFET.

b) $$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = 8\text{ mA}\left(1-\frac{(-2)}{(-4)}\right)^2 = \mathbf{2\text{ mA}}$$

c) $$I_D = 8\text{ mA}\left(1-\frac{(2)}{(-4)}\right)^2 = \mathbf{18\text{ mA}}$$

Q.49 Draw the symbols of D - MOSFETs.

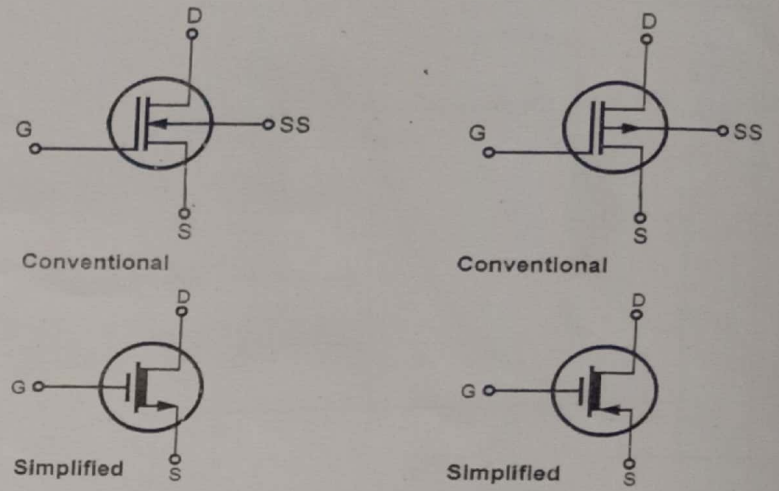
Ans. : • Fig. Q.49.1 shows graphic symbols for a n and p-channel depletion type MOSFET.

See Fig. Q.49.1 on next page.

Q.50 Explain construction of n - channel enhancement type MOSFET.

Ans. : • The Fig. Q.50.1 shows the basic construction of n-channel enhancement type MOSFET.

• Like, depletion type MOSFET, two highly doped n-regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. Q.50.1.



(a) Symbols for n-channel depletion type MOSFETs

(b) Symbols for p-channel depletion type MOSFETs

Fig. Q.49.1 D-MOSFET symbols

• The channel between two n-regions is absent in the enhancement type MOSFET. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

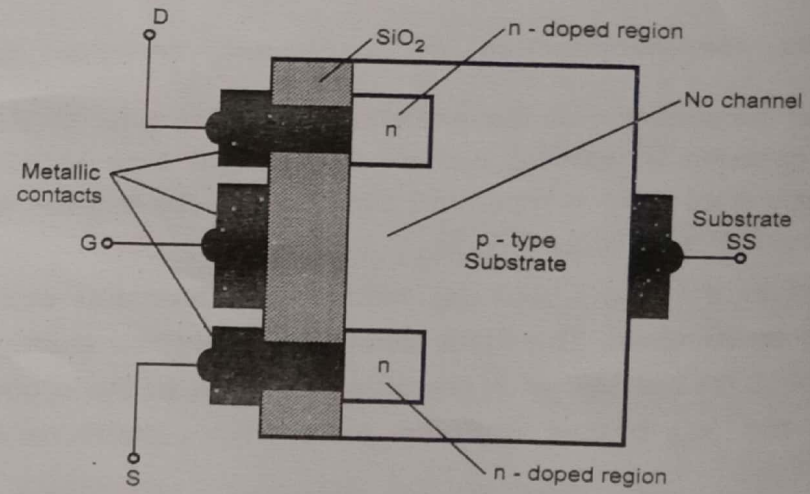


Fig. Q.50.1 n-channel enhancement type MOSFET

- It differs in construction from the depletion MOSFET in that it has no physical channel.

Q.51 Explain the working of n - channel enhancement type MOSFET.

Ans. : • On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows-quite different from the depletion type MOSFET and JFET.

- If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near the SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called **threshold voltage** denoted by V_T.

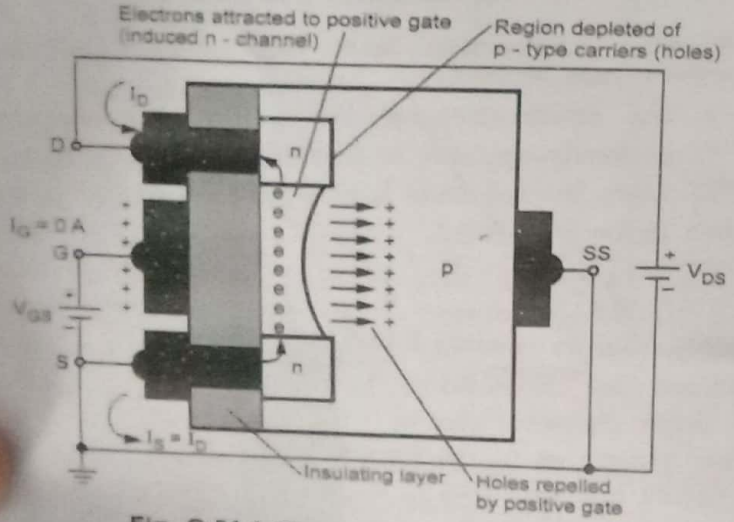


Fig. Q.51.1 Channel formation in the n-channel enhancement type MOSFET

- A positive gate voltage above a threshold value induces a channel and hence the drain current.

- The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel.
- Since the channel does not exist with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an **enhancement type MOSFET**.

Q.52 Draw and explain the drain and transfer characteristics of n - channel E-MOSFET.

Ans. : • Fig. Q.52.1 shows the drain characteristics of an n-channel enhancement type MOSFET. Looking at Fig. Q.52.1 we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET.

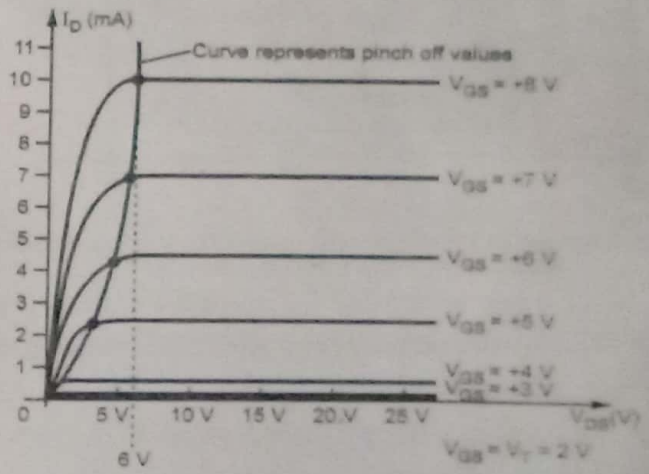


Fig. Q.52.1 Drain characteristics of an n-channel enhancement type MOSFET

Fig. Q.52.2 shows pinch-off process for n-channel enhancement type MOSFET.

- Fig. Q.52.3 shows the transfer characteristic for n-channel enhancement type MOSFET. This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$.

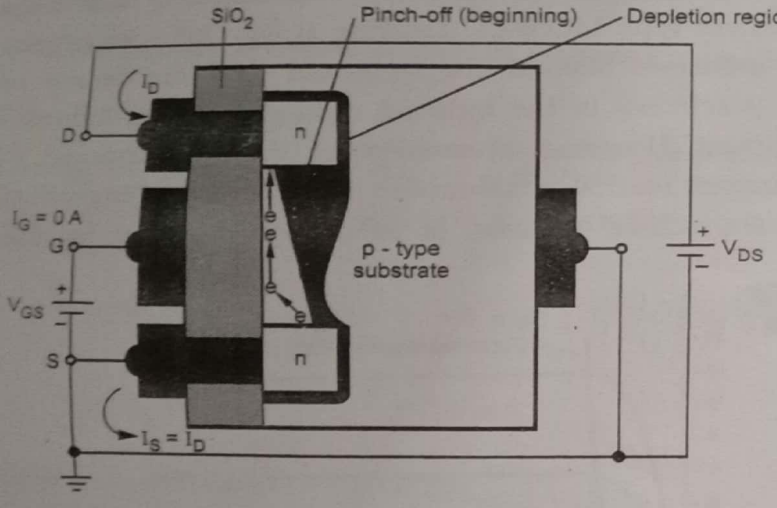


Fig. Q.52.2 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

- For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is nonlinear and it is given as

$$I_D = K(V_{GS} - V_T)^2 \quad \ldots (Q.52.1)$$

- The K term is a constant that is a function of the construction of the device. The value of K can be determined from equation,

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2} \quad \ldots (Q.52.2)$$

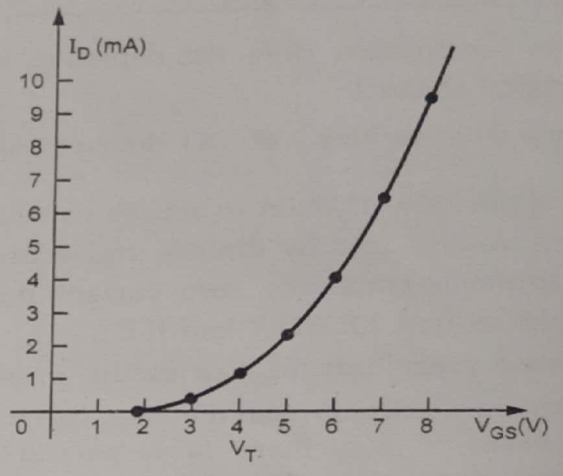


Fig. Q.52.3 Transfer characteristic for n-channel enhancement type MOSFET

Q.53 Explain construction and characteristics of p - channel enhancement type MOSFET.

Ans. : • The construction of the p-channel enhancement type MOSFET is exactly opposite to that of n-channel enhancement type MOSFET. Here, the substrate is of n-type and regions are of p-type as shown in the Fig. Q.53.1.

- As shown in the Fig. Q.53.2 voltage polarities and current directions are reversed. The drain characteristics appear exactly as in the Fig. Q.53.2 but with V_{DS} with negative values, I_D in opposite direction and V_{GS} having opposite polarities as shown in the Fig. Q.53.2.

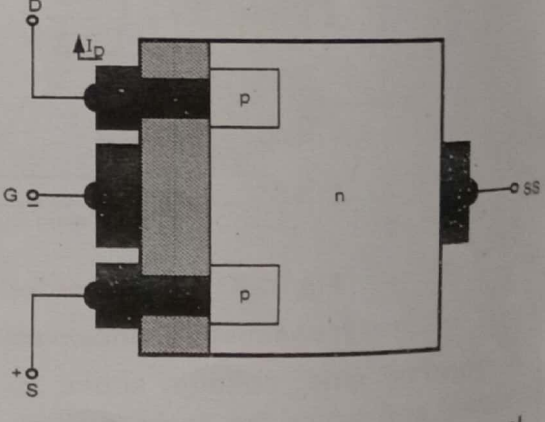


Fig. Q.53.1 Construction of p-channel enhancement type MOSFET

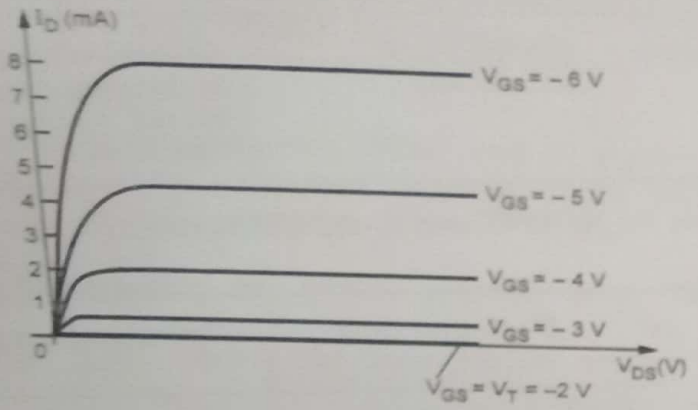


Fig. Q.53.2 Drain characteristics of p-channel enhancement MOSFET

• Fig. Q.53.3 shows the transfer characteristics of p-channel enhancement type MOSFET. In the p-channel enhancement type MOSFET, the transfer characteristic is a mirror image about the I_D axis (y axis) of the transfer characteristics of n-channel depletion type MOSFET, since the V_{GS} is negative.

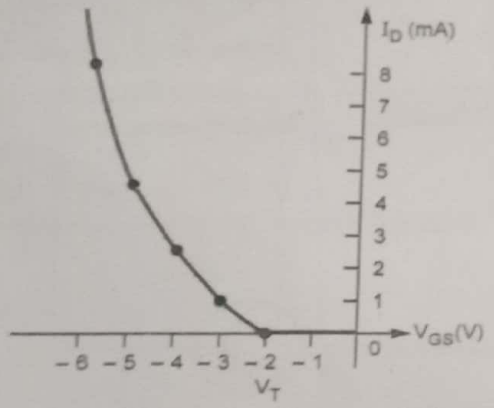


Fig. Q.53.3 Transfer characteristics of p-channel

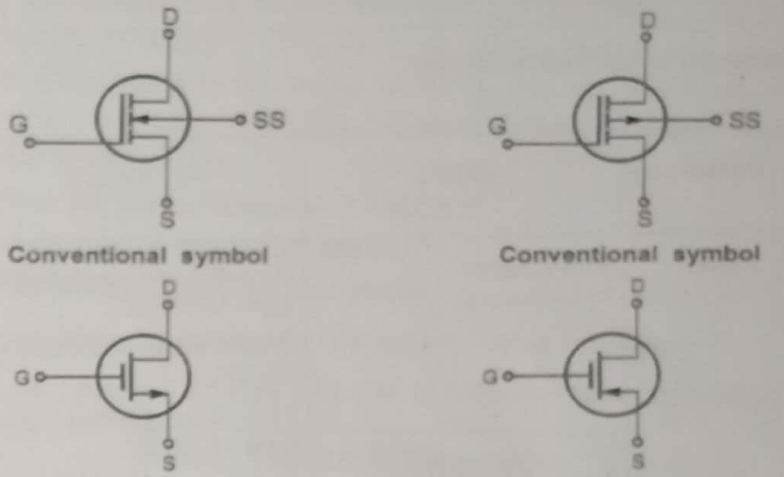
Q.54 Draw the symbols of E-MOSFET.

Ans. : • Fig. Q.54.1 shows graphic symbols for n and p-channel enhancement type MOSFET. (See Fig. Q.54.1 on next page)

Q.55 For a depletion type MOSFET, determine I_D if $V_{GS} = -1$ V, $V_p = -4$ V and $I_{DSS} = 16$ mA.

Ans. :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 16\left(1 - \frac{(-1)}{(-4)}\right)^2 = 9 \text{ mA}$$



(a) Symbols for n-channel enhancement type MOSFETs

(b) Symbols for p-channel enhancement type MOSFETs

Fig. Q.54.1 E-MOSFET symbols

Q.56 For E - MOSFET, determine value of I_D. If $I_{D(ON)} = 4$ mA, $V_{GS(ON)} = 6$ V, $V_T = 4$ V and $V_{GS} = 8$ V.

Ans. :

$$K = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - V_T\right)^2} = \frac{4\times10^{-3}}{(6-4)^2} = 1\times10^{-3} \text{ A/V}^2$$

$$I_D = K(V_{GS} - V_T)^2 = 1\times10^{-3}(8-4)^2 = 16 \text{ mA}$$

Q.57 State the advantages of MOSFET over JFET.

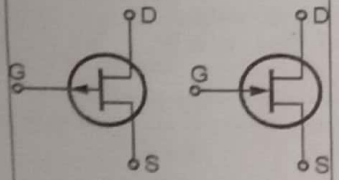
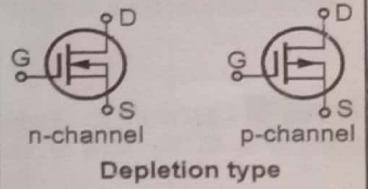
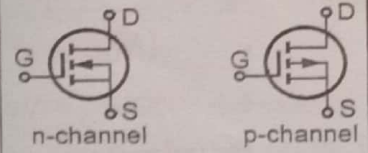
Ans. : The advantages of MOSFET over JFET are :

- Input resistance of MOSFET is higher than JFET.
- JFET can be operated in only depletion mode, however, MOSFET can be operated in enhanced mode as well as depletion mode.
- It can operate with positive as well as negative gate voltages.

5.10 : Comparison between JFETs and MOSFETs

Q.58 Compare JFET and MOSFET.

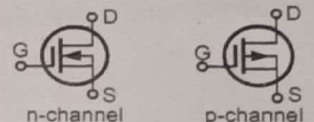
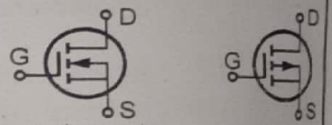
Ans. :

Sr. No.	Parameter	JFET	MOSFET
1.	Types	a) n-channel b) p-channel	A) n-channel depletion type MOSFET B) p-channel depletion type MOSFET C) n-channel enhancement type MOSFET D) p-channel enhancement type MOSFET
2.	Symbols		 Depletion type  Enhancement type
3.	Operation mode	Operated in depletion mode.	Operated in depletion and enhancement mode.
4.	Input impedance	High (> 10 MHz)	Very high (> 10,000 MΩ)
5.	Gate	Gate is not insulated from channel.	Gate is insulated from channel by a layer of SiO_2.

6.	Channel	Channel exists permanently .	Channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET.

Q.59 Compare D - MOSFET and E - MOSFET.

Ans. :

Sr. No	Parameter	Depletion type	Enhancement type
1.	Symbols		
2.	Channel	Exists permanently.	Channel is physically absent. It is induced after application of positive gate voltage above the threshold value for n-channel enhancement type MOSFET and negative gate voltage above threshold value for p-channel enhancement type MOSFET.
3.	Operation	Can be operated in depletion mode as well as enhance mode.	Can only be operated in enhance mode.
4.	Current flow	Drain current flows on application of drain to source voltage, at $V_{GS} = 0$.	Practically no current flows on application of drain to source, at $V_{GS} = 0$. Current flows only when V_{GS} is above threshold level.

5.11 : CMOS Introduction

Q.60 What is CMOS ?

Ans. : • CMOS (Complementary MOS) uses p - channel MOSFET (PMOS) and n - channel MOSFET (NMOS). These MOSFETs are connected as a complementary pair.

Q.61 Draw the structure of CMOS inverter gate. Explain its working.

Ans. : • Fig. Q.61.1 shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to + V_{DD} (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

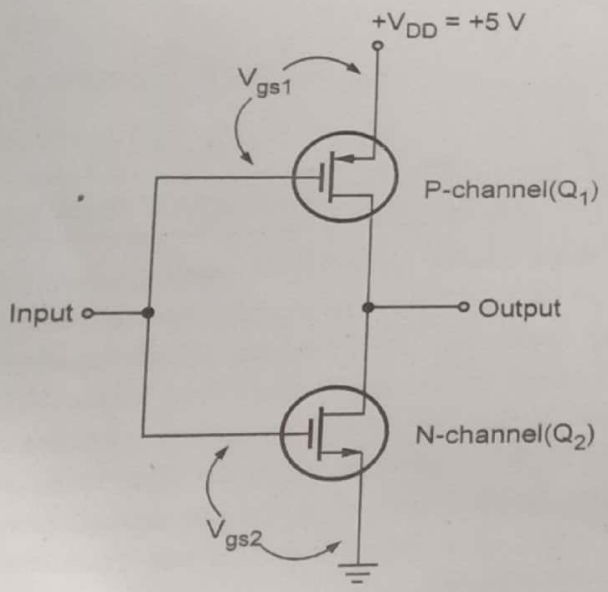


Fig. Q.61.1 CMOS inverter circuit

1. When input is HIGH, the gate of Q_1 (P-channel) is at 0 V relative to the source of Q_1 i.e. $V_{gs_1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (N-channel) is at + V_{DD} relative to its source i.e. V_{gs_2} = + V_{DD}. Thus, Q_2 is ON. This will produce $V_{OUT} \approx 0$ V.

2. When input is LOW, the gate of Q_1 (P-channel) is at a negative potential relative to its source while Q_2 has V_{gs} = 0 V. Thus, Q_1 is ON and Q_2 is OFF. This produces output voltage approximately +V_{DD}.

Q.62 What are the advantages of CMOS ?

Ans. : Advantages of CMOS are :

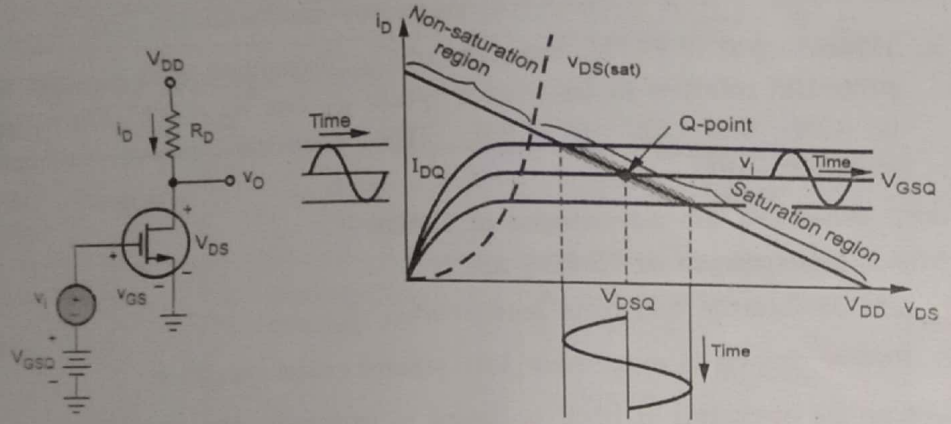
1. CMOS circuits consume less power.
2. Power drawn is extremely low steady - state condition.
3. Can be operated at high voltages to improve noise immunity.

5.12 : EMOSFET Amplifier

Q.63 Explain the operation of CS EMOSFET amplifier with the help of dc load line.

Ans. : • Fig. Q.63.1 shows n-channel, enhancement mode MOSFET common-source circuit with a time-varying (a.c.) voltage source in series with the d.c. source. We assume the time-varying input signal is sinusoidal.

- Fig. Q.63.1 shows the MOSFET characteristics, d.c. load line, and Q-point, where the d.c. load line and Q-point are functions of v_{GS}, V_{DD}, R_D and the MOSFET parameters.
- For the output voltage to be a linear function of the input voltage, the MOSFET is biased in the saturation region.
- The Fig. Q.63.1 (b) shows sinusoidal variations in the gate-to-source voltage, drain current and drain-to-source voltage, as a result of the sinusoidal source v_i.
- The total gate-to-source voltage is the sum of V_{GSQ} and v_i.
- As v_i increases, the instantaneous value of v_{GS} increases, and the bias point moves up the load line. A larger value of v_{GS} means a larger drain current and a smaller value of v_{DS}.



(a) NMOS common-source circuit with time varying signal source in series with gate d.c. source

(b) Common-source transistor characteristics, d.c. load line, and sinusoidal variation in gate-to-source voltage, drain current, and drain-to-source voltage

Fig. Q.63.1

Q.64 For the circuit shown in Fig., find V_{GS}, I_D, g_m and V_{out}. Assume $K = 104 \times 10^{-3}\ A/V^2$, $I_{D(on)} = 600$ mA and $V_T = 2.1V$

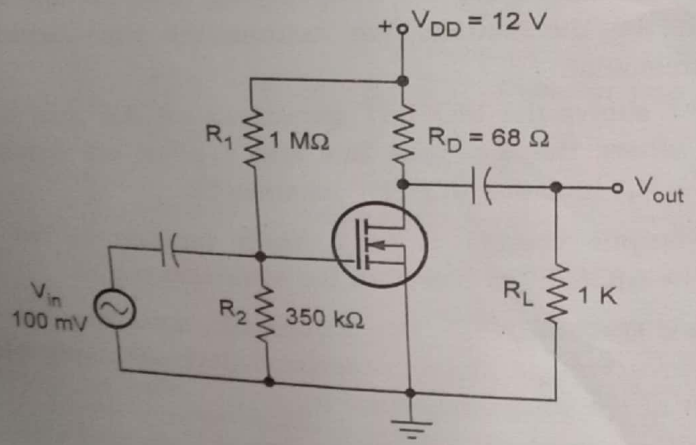


Fig. Q.64.1

Ans. : $V_{GS} = V_G = \dfrac{350\ K}{350\ K + 1\ M\Omega} \times 12 = 3.11\ V$

$I_D = K(V_{GS} - V_T)^2 = 104 \times 10^{-3} (3.11 - 2.1)^2 = 106\ mA$

We know that,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ and } I_D = K[V_{GS} - V_T]^2$$

$$\therefore \quad g_m = 2K[V_{GS} - V_T]$$

$$= 2 \times 104 \times 10^{-3} [3.11 - 2.1] = 210\ mS$$

The voltage gain of the CS MOSFET amplifier is given by

$$A_V = g_m r_d \qquad \text{where } r_d = R_D || R_L$$

$$= 68\ \Omega\ ||\ 1\ K\ \Omega = 63.7\ \Omega$$

$$\therefore \quad A_V = 210 \times 10^{-3} \times 60.7\Omega = 13.4$$

and $V_{out} = A_V V_{in} = 13.4 \times 100\ mV = 1.34\ mV$

5.13 : MOSFET Testing

Q.65 Write a note on MOSFET testing.

Ans. : • MOSFET devices require special care when being tested for proper operation. The thin layer of silicon dioxide between the gate and channel can be easily destroyed when VGS exceeds VGS(max). Because of the insulated gate, along with the channel construction, testing MOSFET devices with an ohmmeter or DMM is not very effective. A good way to test these devices is with a semiconductor curve tracer. If a curve tracer is not available, special test circuits can be constructed.

- Fig Q.65.1 shows a circuit capable of testing both depletion-mode and enhancement-mode MOSFETs. By changing the voltage level and polarity of V1, the device can be tested in either depletion or enhancement modes of operation.

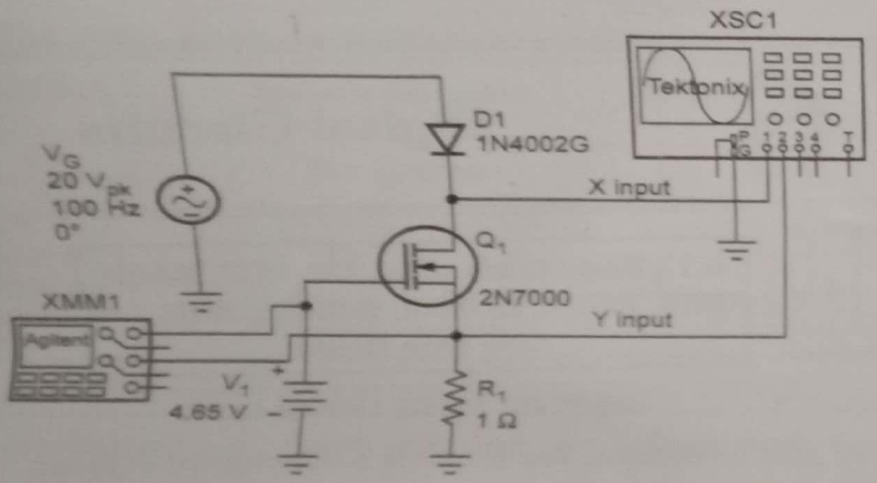


Fig. Q.65.1

5.14 : Reading Datasheet for FET and MOSFFET

Q.66 Write a note on FET datasheets.

Ans. : • FET datasheets contain a host of different parameters and specifications which define the performance of the particular FET type.

- When developing a new circuit or replacing an existing FET it is important to understand the different parameters and specifications that appear in the datasheets so that the correct device can be chosen and used.
- All the specifications and parameters are important in different applications. Also dependent upon the device, the FET datasheets may quote different parameters which are relevant to the particular for which the device is intended.

Major FET datasheet specifications and parameters are :

- **Gate source voltage, V_{GS} :** The FET parameter V_{GS} is the rating for the maximum voltage that can be tolerated between the gate and source terminals.

- **Drain-Source Voltage, V_{DSS} :** This is a rating for the maximum drain-source voltage that can be applied without causing avalanche breakdown. The parameter is normally stated for the case where the gate is shorted to the source and for a temperature of 25 °C.

Gate reverse leakage current, I_{gss} :

- **Threshold voltage $V_{GS(TH)}$:** The threshold voltage $V_{GS(TH)}$ is the minimum gate voltage that can form a conducting channel between the source and the drain. It is normally quoted for a given source drain current.
- **Drain current at zero gate voltage, I_{dss} :** This FET parameter is the maximum continuous current the device can carry with the device fully on. Normally it is specified for a particular temperature, typically 25 °C.
- **Gate source cut-off voltage, $V_{GS(off)}$:** The gate source cut-off voltage is really a turn-off specification.

Forward transconductance, G_{fs} :

- **Input capacitance, C_{iss} :** The input capacitance parameter for a FET is the capacitance that is measured between the gate and source terminals with the drain shorted to the source for AC signals.
- **Drain-source on resistance, $R_{ds(on)}$:** With the FET turned hard on, this is the resistance in ohms exhibited across the channel between the drain and source
- **Power dissipation, P_{tot} :** This FET specification details the maximum continuous power that the device can dissipate.
- Along with these parameters such as **Forward transconductance and Gate reverse leakage current are also specified in the FET datasheets.**

Q.67 State the important specification of MOSFET.

Ans. : Important Specification of MOSFET are : Operating Junction and Storage Temperature Range, Junction-to-Case thermal resistance $R_{\theta JC}$, thermal resistance , Gate Charge, Drain-to-Source Breakdown Voltage, Static Drain-to-Source On-Resistance $R_{DS(on)}$, Gate Threshold Voltage $V_{GS(th)}$, Turn-on time, Rise time, Turn-off time and Fall times. .

END...

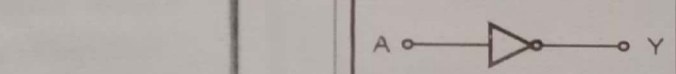
6 Digital Circuits

6.1 : Basic Gates, AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR, Building AND, OR Gate with Diodes

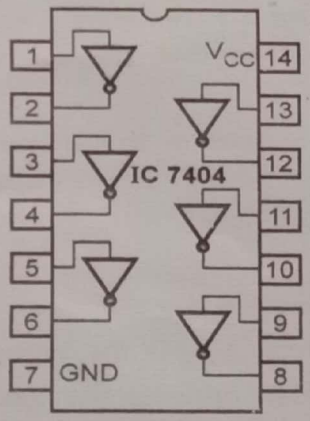
Important Points to Remember

NOT gate (inverter) : The output is a complement of input.

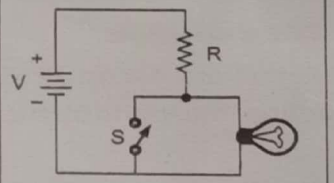
Logic diagram (symbol)



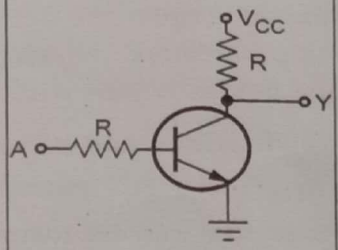
Pin diagram



Switch equivalent



Input	Output
Switch open (Low)	Lamp ON (High)
Switch close (High)	Lamp OFF (Low)



Truth table

Input	Output
A	Y
0	1
1	0

Boolean Expression

$Y = \overline{A}$

Application :

Used to complement (invert) digital signal.

uffer : The output is same as input.

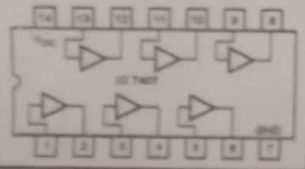
Symbol

Application : It is used to increase output driving capacity.

Boolean expression

$Y = A$

Pin diagram



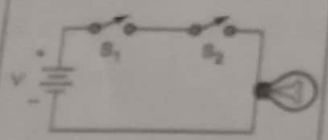
Truth table

Input	Output
A	Y
0	0
1	1

ND gate : The output is high only when all inputs are high.

Logic diagram (symbol)

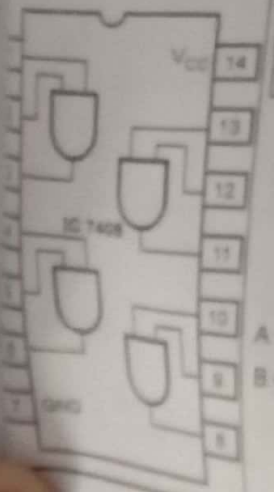
Switch equivalent



Truth table

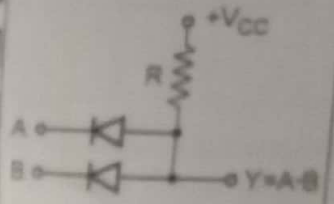
Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0

Pin diagram



Input		Output
S_1	S_2	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp OFF (Low)
Close (High)	Open (Low)	Lamp OFF (Low)
Close (High)	Close (High)	Lamp ON (High)

Diode equivalent



Boolean expression

$Y = A \cdot B$

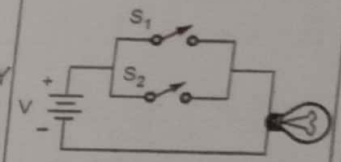
Application :

Used to implement logical AND operation.

OR gate : The output is high when any of the inputs is high.

Logic diagram (symbol)

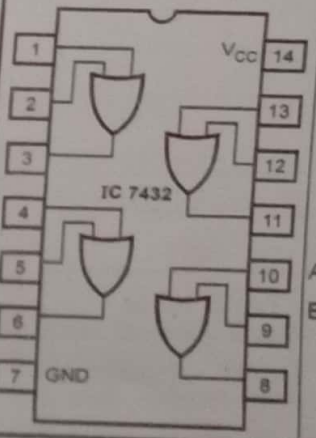
Switch equivalent



Truth table

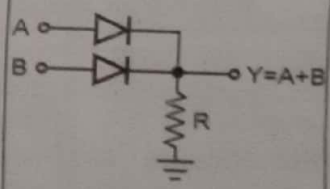
Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

diagram



Input		Output
S_1	S_2	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp ON (High)
Close (High)	Open (Low)	Lamp ON (High)
Close (High)	Close (High)	Lamp ON (High)

Diode Equivalent



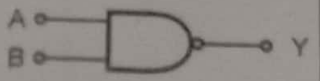
Boolean Expression

$Y = A + B$

Application : Used to implement logical OR operation.

NAND gate : The output is high only when one of the inputs is low.

Symbol

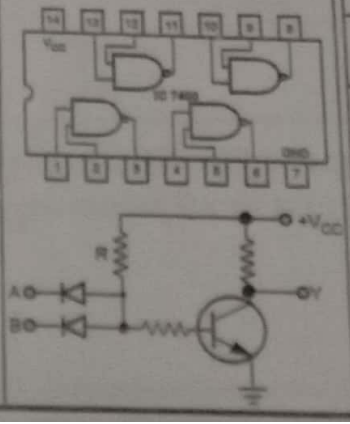


Application : It can be used to implement any digital circuit.

Boolean expression

$Y = \overline{A \cdot B}$

Pin diagram

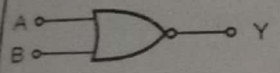


Truth table

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate : The output is high when all the inputs are low.

Symbol

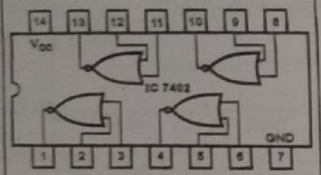


Application : It can be used to implement any digital circuit.

Boolean expression

$Y = \overline{A + B}$

Pin diagram

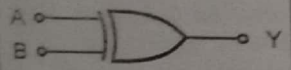


Truth table

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Exclusive OR (EX-OR) gate : The output is high only when odd number of inputs are high.

Symbol

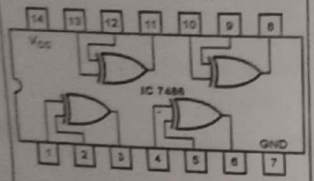


Application : It is used to implement magnitude comparator, gray code converter, adder/subtractor circuits, parity generator, modulo-2 adder, etc.

Boolean expression

$Y = A \oplus B$

Pin diagram

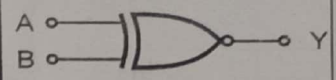


Truth table

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive NOR (EX-NOR) gate : The output is high only when even number of ones at the input or all inputs are high.

Symbol

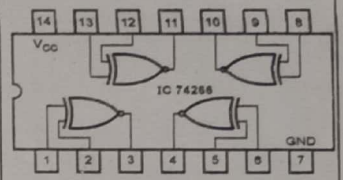


Application : It is used to implement even parity generator, comparator, even parity checker, etc.

Boolean expression

$Y = \overline{A \oplus B}$

Pin diagram



Truth table

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Q.1 The voltage waveforms shown in Fig. Q.1.1 are applied at the inputs of 2-input AND and EX-OR gates. Determine the output waveform in each case.

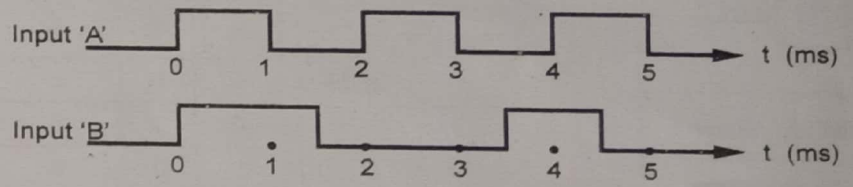


Fig. Q.1.1

Ans. :

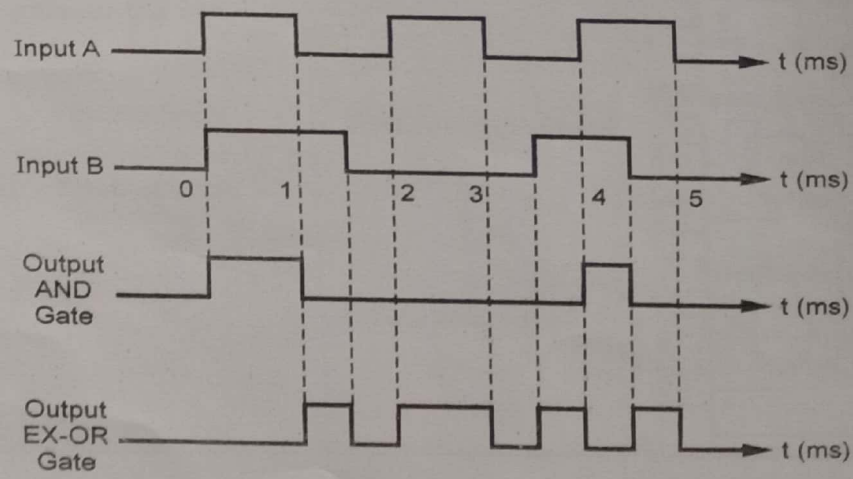


Fig. Q.1.1 (a)

2 Write down the truth table for 3-input EX-OR gate.

ns. : The output is logic 1 when odd number of input(s) is logic 1.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table Q.2.1

.3 Make truth table for a 3 input :
) AND gate 2) OR gate 3) NAND gate 4) NOR gate.

ns. :

A	B	C	Y
)	0	0	0
)	0	1	0
)	1	0	0
)	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 input AND

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3 input OR

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

3 input NAND

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

3 input NOR

Fig. Q.3.1 Truth table

.4 Prove that a positive logic NAND is equivalent to a negative ogic NOR operation and vice versa.

Ans. :

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for NAND gate with positive logic

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth table for NOR gate with positive logic

A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

Truth table for NAND gate with negative logic

A	B
1	1
1	0
0	1
0	0

Truth table NOR gate w negative log

The truth tables for positive logic NAND gate and negative log NOR gates are equivalent and vice versa.

6.2 : Digital Logic Families

Q.5 What is logic family ? Give the classification of logic families.
Ans. : A digital logic family is a group of compatible devices with the same logic levels and supply voltages. According to components used in the logic family, digital logic families are classified as shown in the Fig. Q.5.1.

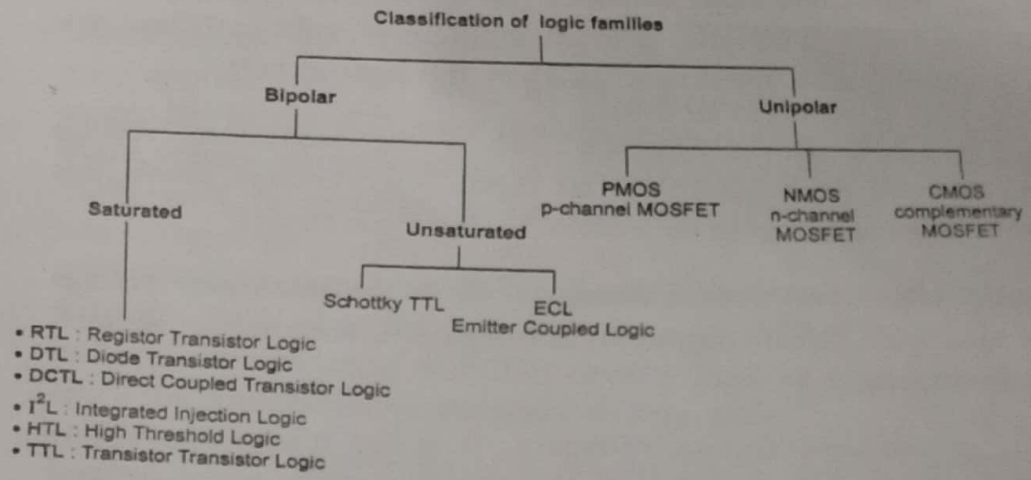


Fig. Q.5.1 Classification of logic families

Q.6 Define fan-in and fan-out.

OR Define and explain fan-out.

OR Define and explain propagation delay.

OR Define noise margin.

OR Define figure of merit.

Ans. : Propagation Delay : The propagation delay of a gate is basically the time interval between the application of an input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa.

Power Dissipation : The amount of power that an IC dissipates is determined by the average supply current, I_{CC}, that it draws from the V_{CC} supply. It is the product of I_{CC} and V_{CC}.

Current and Voltage Parameter

$V_{IH\,(min)}$- High-Level Input Voltage : It is the minimum voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

$V_{IL\,(max)}$- Low-Level Input Voltage : It is the maximum voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

$V_{OH\,(min)}$- High-Level Output Voltage : It is the minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.

$V_{OL\,(max)}$- Low-Level Output Voltage : It is the maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

I_{IH}- High-Level Input Current : It is the current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL}- Low-Level Input Current : It is the current that flows into an input when a specified low-level voltage is applied to that input.

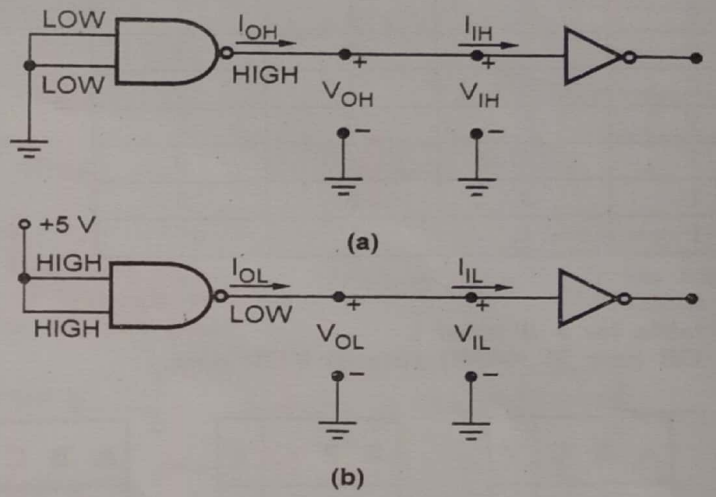


Fig. Q.6.1 Currents and voltages in the two logic states

I_{OH}- High-Level Output Current : It is the current that flows from an output in the logical 1 state under specified load conditions.

I_{OL}- Low-Level Output Current : It is the current that flows from an output in the logical 0 state under specified load conditions.

Noise Margin : The **noise immunity** of at a logic circuit refers to the circuit's ability to tolerate the noise without causing spurious changes in the output voltage. To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept at a few fraction of volts below $V_{OH(min)}$ and voltage level $V_{IL(max)}$ is kept above $V_{OL(max)}$, at the design time.

V_{NH} is the difference between the lowest possible HIGH output, $V_{OH(min)}$ and the minimum voltage, $V_{IH(min)}$ required for a HIGH input. This voltage difference, V_{NH} is called high-state noise

margin. Similarly, we have low-state noise margin. It is the voltage difference between the largest possible low output, $V_{OL(max)}$ and the maximum voltage, $V_{IL(max)}$ required for a LOW input.

In short we can write as,

$$V_{NH} = V_{OH(min)} - V_{IH(min)} \quad \text{and}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

Fan-in and Fan-out : The maximum number of inputs of several gates that can be driven by the output of a logic gate is decided by the parameter called **fan-out**. In general, the fan-out is defined as the maximum number of inputs of the same IC family that the gate can drive maintaining its output levels within the specified limits.

The **fan-in** of a digital logic gate refers to the number of inputs.

Speed Power Product (Figure of Merit)

- In general, for any digital IC, it is desirable to have shorter propagation delays (higher speed) and lower values of power dissipation. There is usually a trade-off between switching speed and power dissipation in the design of a logic circuit i.e. speed is gained at the expense of increased power dissipation. Therefore, a common means for measuring and comparing the overall performance of an IC family is the **Speed-Power Product (SPP). It is also called Figure of Merit.**

Operating Temperature Range

- It is the temperature range specified by the logic family within which devices are guaranted to work reliably.

Power Supply Requirements

Power supply requirements differ from logic family to family. For example, it is 5 V for TTL family and 3-15 volts for CMOS family. Further more, power supply tolerance also depends on logic family. For example, for 74 series TTL family it is ± 0.25 V and for 54 series TTL family it is ± 0.5 V.

Q.7 Draw and explain the operation of 2-input RTL NOR Ga

Ans. : • *RTL circuits consist of resistors and transistors. Fi shows 2-input RTL NOR gate. As shown in the Fig. Q.7.1, e of both the transistors are connected to a common grou collectors of both transistors are tied through a common c resistor R_C to a supply voltage V_{CC} . The resistor R_C is com known as* **passive pull-up** *resistor.*

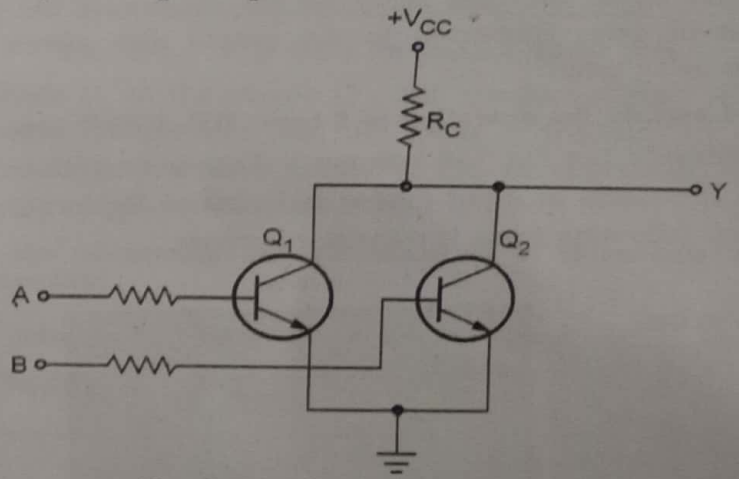


Fig. Q.7.1 2-input RTL NOR gate

Circuit operation :

- Inputs representing logic levels are applied at A and B terminals. In the RTL gate the input voltage corresponding to LOW level is required to be low enough for the corresponding transistor to be cut off. Similarly, the input voltage corresponding to HIGH level should be high eno drive the corresponding transistor to saturation.

A	B	Y
0	0	1
0	1	0
1	0	0

Table Q.7.1 Truth table for 2 NOR gate

- When both the inputs are Low, transistors Q_1 and Q_2 are and the output is HIGH. A HIGH level on any input dri

corresponding transistor to saturation causing the output to go LOW. Table Q.7.1 shows the truth table for 2-input NOR gate.

- We know that, the saturation voltage, $V_{CE\ (sat)}$ for transistor is approximately 0.2 V. Therefore, for RTL gates the LOW level output voltage is 0.2 V. In RTL a HIGH level output voltage depends on the number of gates connected to the output. As number of gates connected to the output increases, output voltage decreases. This is the deciding factor for the fan-out of the gate. The number of gates connected to the output also affects the propagation delay time.

Q.8 Draw and explain the operation of 2-input DTL NAND gate.

Ans. : DTL circuit : The Fig. Q.8.1 shows a discrete circuit for DTL NAND gate. It consists of input diodes and resistor R_D forming an AND gate and following them is transistor inverter.

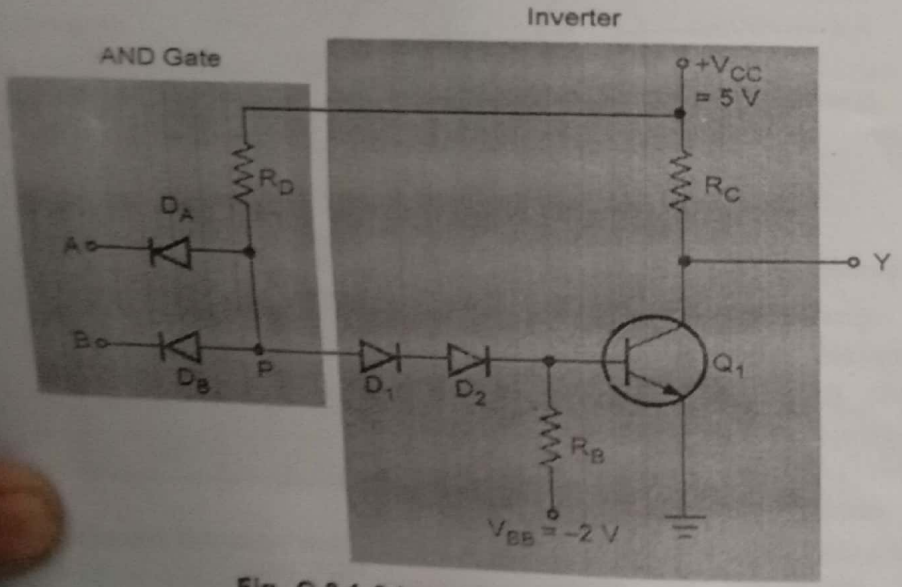


Fig. Q.8.1 2-input DTL NAND gate

Circuit operation :

- When both inputs are LOW, diode D_A and D_B conduct resulting 0.7 volts at point P. This 0.7 voltage at point is not sufficient to drive transistor Q_1. Therefore, Q_1 is cut off giving output voltage

$V_o = V_{CC}$ logic 1. A LOW level on any input cause corresponding diode to conduct resulting voltage at point P = 0.7 V.

- This causes transistor to remain in cut-off and the output voltage is equal V_{CC} = logic 1. When both inputs are logic HIGH, diodes D_A and D_B are reversed biased. This causes the base current of transistor Q_1 to flow through R_D, D_1, D_2 and the base of the transistor Q_1. This drives transistor Q_1 in saturation giving output voltage = $V_{CE\ (sat)}$ = 0.2 V = logic 0.
- For driving transistor Q_1 is saturation we require more than 2.1 V (V_{D_1} (0.7) + V_{D_2} (0.7) + 0.7 (V_{BE})) at point P to drive transistor in saturation. Therefore, we can say that due to diodes D_1 and D_2 we need increased voltage level to drive transistor in saturation. This improves the noise margin for DTL gate.
- When A and B inputs are HIGH, transistor Q_1 is driven in saturation and its base to emitter junction capacitance is charged. Now if any of the input goes low, voltage at point P becomes 0.7 V and transistor Q_1 will try to come out of saturation. To drive transistor from saturation to cut-off it is necessary to discharge the stored charge on the internal capacitance. The resistance, R_B provides a discharge path for the charged stored in the transistor. Resistor R_B is connected to the – 2 V supply to increase the rate of discharge.

Q.9 With neat circuit diagram explain the operation of two-input TTL NAND gates.

Ans. : The Fig. Q.9.1 (a) shows the circuit diagram of 2-input NAND gate. Its input structure consists of multiple-emitter transistor and output structure consists of totem-pole output. Here, Q_1 is an NPN transistor having two emitters, one for each input to the gate. Although this circuit looks complex, we can simplify its analysis by using the diode equivalent of the multiple-emitter transistor Q_1, as shown in Fig. Q.9.1 (b). Diodes D_2 and D_3 represent the two E-B junctions of Q_1 and D_4 is the collector-base (C-B) junction.

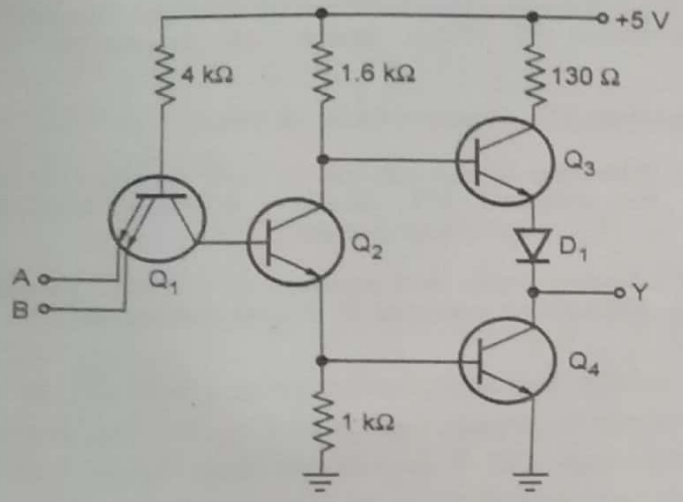


Fig. Q.9.1 (a) Two input TTL NAND gate

he input voltages A nd B are either LOW deally grounded) or IGH (ideally +5 volts). either A or B or both re low, the rresponding diode onducts and the base f Q_1 is pulled down to pproximately 0.7 V. his reduces the base oltage of Q_2 to almost ero. Therefore, Q_2 cuts off. With Q_2 open , Q_4 goes into cut-off nd the Q_3 base is pulled HIGH. Since Q_3 acts as an emitter ollower, the Y output is pulled up to a HIGH voltage. On the ther hand, when A and B both are HIGH, the emitter diode of Q_1 re reversed biased making them off. This causes the collector iode D_4 to go into forward conduction. This forces Q_2 base to go IGH. In turn, Q_4 goes into saturation, producing a low output. able Q.9.1 summarizes all input and output conditions.

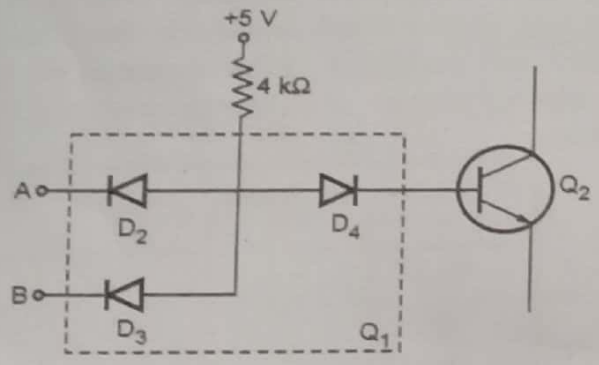


Fig. Q.9.1 (b) Diode equivalent for Q_1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table Q.9.1 Truth table for 2-input NAND gate

Without diode D_1 in the circuit, Q_3 will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of Q_3 reverse-biased. In this way, only Q_4 conducts when the output is low.

Q.10 Give the advantages and disadvantages of totem-pole output stage arrangement.

OR Give comparison between totem-pole and open colletor outputs.

Ans. :

Sr. No.	Totem-pole	Open collector
1.	Output stage consists of pull-up transistor (Q_3), diode resistor and pull-down transistor (Q_4).	Output stage consists of only pull-down transistor.
2.	External pull-up resistor is not required.	External pull-up resistor is required for proper operation of gate.
3.	Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique.
4.	Operating speed is high.	Operating speed is low.

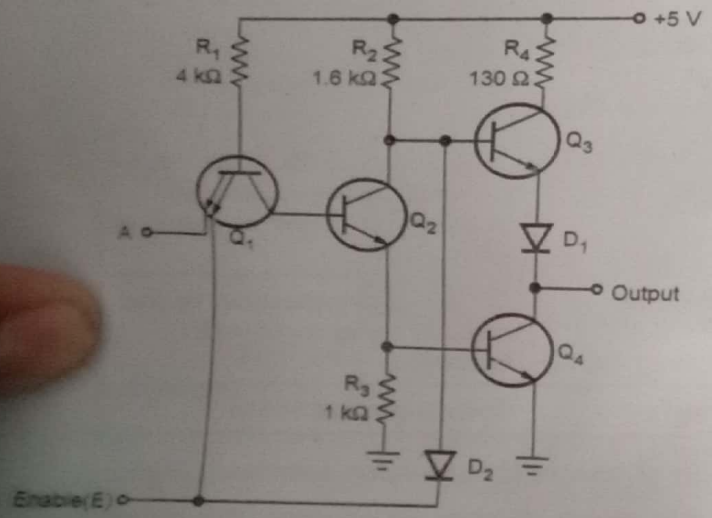
Table Q.10.1 Comparison of totem-pole and open collector output

Q.11 Draw and explain the circuit diagram of tri-state TTL NAND gate.

Ans. : The tristate configuration is a third type of TTL output configuration. It utilizes the high-speed operation of the totem-pole arrangement while permitting outputs to be wired-ANDed (connected together). It is called tristate TTL because it allows three possible output stages : HIGH, LOW and high-impedance.

Fig. Q.11.1 shows the simplified circuit for tristate inverter. It has two inputs A and E.

A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state of the transistor Q_1 (either ON or OFF) depends on the logic input A, and the additional component diode is open circuited as its cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input A, the base-emitter junction of Q_1 is forward biased and as a result it turns ON. This shunts the current through R_1 away from Q_2 making it OFF. As Q_2 is OFF, there is no sufficient drive for Q_4 to conduct and hence Q_4 turns OFF. The LOW at ENABLE input also forward-biases diode D_2, which shunt the current away from the base of Q_3, making it OFF. In this way, when ENABLE input is LOW, both transistors are OFF and output is at high impedance state.



A	E	Output
0	1	1
1	1	0
X	0	Floating

Truth table

Fig. Q.11.1 Tristate TTL inverter

Q.12 Explain the following characteristics of TTL logic families : i) Power dissipation ii) Noise margin iii) Propagation delay iv) Fan out.

OR Explain standard TTL characteristics in detail.

OR Define the following terms related to logic families. Mention typical values for standard TTL family : i) Power dissipation ii) Fan-in iii) V_{IL}, V_{OH} iv) Noise margin.

OR Define the following terms and mention its standard values for TTL family : i) Voltage parameters ii) Power dissipation iii) Fan out.

Ans. : Supply voltage and temperature range : Both the 74 series and 54 series operate on supply voltage of 5 V. The 74 series works reliably over the range 4.75 V to 5.25 V, while the 54 series can tolerate a supply variation of 4.5 to 5.5 V.

Voltage levels and noise margin : Table Q.12.1 shows the input and output logic voltage levels for the standard 74 series. The minimum and maximum values shown in the Table Q.12.1 are for worst case conditions of power supply, temperature and loading conditions.

Voltages	Minimum	Typical	Maximum
V_{OL}	–	0.2	0.4
V_{OH}	2.4	3.4	–
V_{IL}	–	–	0.8
V_{IH}	2.0	–	–

Table Q.12.1 Voltage levels

For TTL, Low state noise margin, V_{NL} and high state noise margin, V_{NH} both are equal and 0.4 V.

Power dissipation and propagation delay : A standard TTL gate has an average power dissipation of about 10 mW.

Fan-out : A standard TTL output can typically drive 10 standard TTL inputs. Therefore, standard TTL has fan-out 10.

Q.13 Draw the structure of CMOS inverter gate. Explain its working.

Ans. : Fig. Q.13.1 shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to + V_{DD} (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

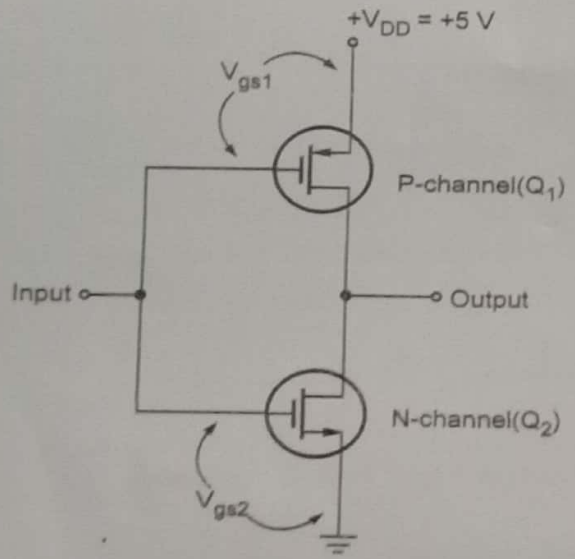
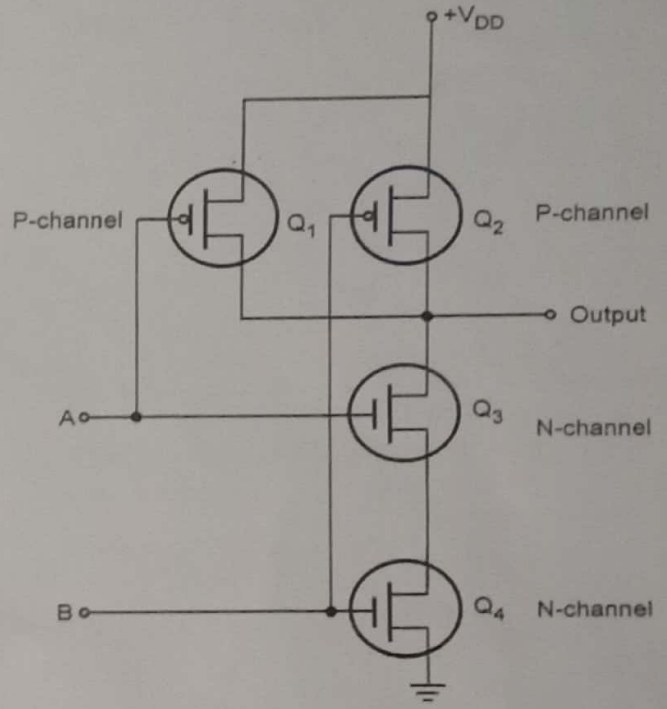


Fig. Q.42.1 CMOS inverter circuit

1. When input is HIGH, the gate of Q_1 (P-channel) is at 0 V relative to the source of Q_1 i.e. $V_{gs_1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (N-channel) is at + V_{DD} relative to its source i.e. V_{gs_2} = + V_{DD}. Thus, Q_2 is ON. This will produce V_{OUT} = 0 V.
2. When input is LOW, the gate of Q_1 (P-channel) is at a negative potential relative to its source while Q_2 has V_{gs} = 0 V. Thus, Q_1 is ON and Q_2 is OFF. This produces output voltage approximately $+V_{DD}$.

Q.14 Explain with neat diagram two input CMOS NAND gate.

Ans. : • Fig. Q.14.1 shows CMOS 2-input NAND gate. It consists of two P-channel MOSFETs, Q_1 and Q_2, connected in parallel and two N-channel MOSFETs, Q_3 and Q_4 connected in series.



Schematic

Fig. Q.14.1 CMOS NAND gate

• Here, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to + V_{DD}. Thus, Q_1 and Q_2 are both ON. Since the gate - to - source voltages of Q_3 and Q_4 (N-channel MOSFETs) are both 0 V, those MOSFETs are OFF. The output is therefore connected to $+V_{DD}$ (HIGH) through Q_1 and Q_2 and is disconnected from ground. When A = 0 and B = $+V_{DD}$. Q_1 is on because $V_{GS_1} = -V_{DD}$ and Q_4 is ON because $V_{GS_4} = +V_{DD}$. MOSFETs Q_2 and Q_3 are off because their gate-to-source voltages are 0 V. Since Q_1 is ON and Q_3 is OFF, the output is connected to + V_{DD} and it is disconnected from ground. When A = $+V_{DD}$ and B = 0 V, the situation is similar (not shown); the output is connected to + V_{DD} through Q_2 and it is disconnected from ground because Q_4 is OFF. Finally, when both inputs are high (A = B = $+V_{DD}$), MOSFETs Q_1 and Q_2 are both OFF and Q_3 and Q_4 are both ON. Thus, the

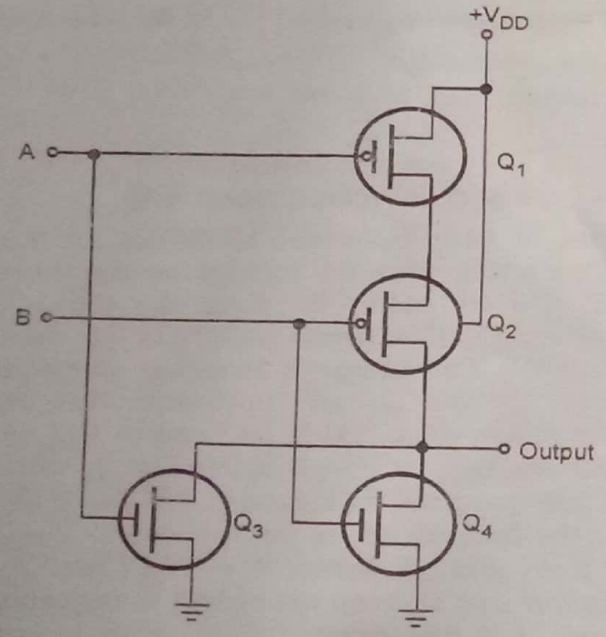
output is connected to the ground through Q_3 and Q_4 and it is disconnected from $+V_{DD}$. The Table Q.14.1 summarizes the operation of 2-input CMOS NAND gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table Q.14.1 Truth table of NAND gate

Q.15 Explain with neat diagram two input CMOS NOR gate.

Ans. : • Fig. Q.15.1 (a) shows 2-input CMOS NOR gate. Here, P-channel MOSFETs Q_1 and Q_2 are connected in series and N-channel MOSFETs Q_3 and Q_4 are connected in parallel.



Schematic

Fig. Q.15.1 CMOS NOR gate

• The Table Q.15.1 summarizes the operation of 2-input NOR gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table Q.15.1 Truth table for NOR gate

Q.16 Give the comparison between various logic families.

OR Compare TTL, CMOS and ECL.

Ans. :

Parameter	RTL	DTL	TTL	CMOS
Components used	Resistors and transistor	Resistor, diode and transistor	Resistor, diode and transistor	N channel and P channel MOSFET
Circuit	Simple	Moderate	Complex	Moderate
Noise margin	Poor	High	Medium	High
Fan-out	Low (4)	Medium (8)	More (10)	50
Power dissipation in mW per gate	30	8 - 12	10	0.1
Basic gate	NOR	NAND	NAND	NAND/NOR
Propagation delay in ns	12	30	10	70
Speed power product (PJ)	144	300	100	0.7

Applications	Absolute	Absolute	Laboratory instruments.	Due to low power consumption they are used in portable instrument where battery supply is used.

END...

SOLVED MODEL QUESTION PAPER

[AS PER R-18 PATTERN]

Time : 3 Hours] **[Total Marks : 70**

Instructions :

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

Q.1 a) *Compare ideal and practical diode.* **(Refer Q.8 of chapter - 1)**

b) *Draw and explain V-I characteristics of a p-n junction diod* **(Refer Q.6 of chapter - 1)**

c) *Draw a positive clamper and explain its working along the waveforms.* **(Refer Q.50 of chapter - 1)**

Q.2 a) *Explain the construction of npn and pnp transistor.* **(Refer Q.6 of chapter - 2)**

b) *Derive the relationship between* α_{dc} *and* β_{dc}. **(Refer Q.26 of chapter - 2)**

c) *Draw and explain the input characteristics of configuration.* **(Refer Q.19 of chapter - 2)**

OR

c) *With a neat diagram explain the output characteristics transistor in CE configuration.* **(Refer Q.33 of chapter - 2)**

Q.3 a) *What is thermal runaway ?* **(Refer Q.69 of chapter -**

b) *Write a note on sixteen segment display.* **(Refer Q.23 of chapter - 3)**

c) *What is d.c. load line ? Derive its equation for amplifier.* **(Refer Q.43 of chapter - 2)**

OR

Q.3 a) *Calculate the Q point values (*I_C *and* V_{CE}*) for the circ Fig. 1.* **(Refer Q.58 of chapter - 2)**

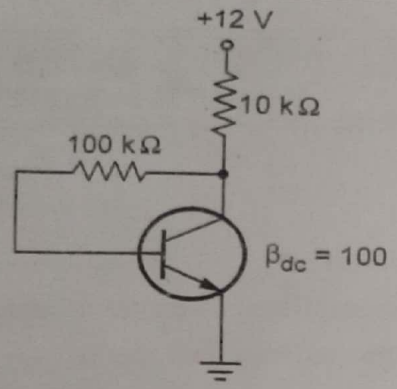


Fig. 1

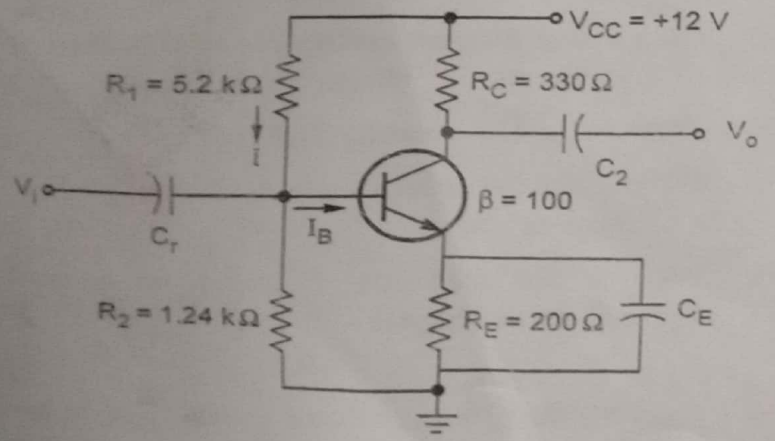
b) *Draw and explain the operation of CE amplifier circuit with neat waveform.* **(Refer Q.17 of chapter - 4)** **[4]**

c) *Explain the operation of BJT as a switch.*
(Refer Q.71 of chapter - 2) **[7]**

Q.4 a) *Explain the way to eliminate the effect of ac degeneration in collector to base bias circuit.* **(Refer Q.5 of chapter - 4)** **[3]**

b) *What is varactor diode ? Explain how it can be used as variable capacitance with the help of characteristics. State its applications.*
(Refer Q.15 of chapter - 3) **[4]**

c) *Draw the dc and ac load lines for the transistor circuit shown in Fig. 2.* **(Refer Q.7 of chapter - 4)** **[7]**



OR

Q.4 a) *List important features of FET.* **(Refer Q.2 of chapter**

b) *For the circuit shown in the Fig. 3 Calculate :*
a) V_{GSQ}, *b)* I_{DQ}, *c)* V_{DSQ}, *d)* V_D
(Refer Q.16 of chapter - 5)

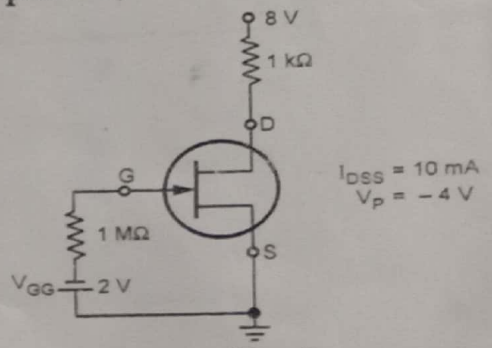


Fig. 3

c) *Explain the drain characteristics for an n-channel*
(Refer Q.9 of chapter - 5)

Q.5 a) *Write down the truth table for 3-input EX-OR ga*
(Refer Q.2 of chapter - 6)

b) *Explain the working of n-channel FET.*
(Refer Q.6 of chapter - 5)

c) *Derive the expressions for input impeda impedance, voltage gain, current gain and power gain for c circuit.* **(Refer Q.18 of chapter - 4)**

OR

Q.5 a) *Explain JFET as multiplexer.* **(Refer Q of cha**

b) *Draw the structure of CMOS inverter gate. working.* **(Refer Q.13 of chapter - 6)**

c) *Explain the working of n - channel enhan MOSFET.* **(Refer Q.51 of chapter - 5)**